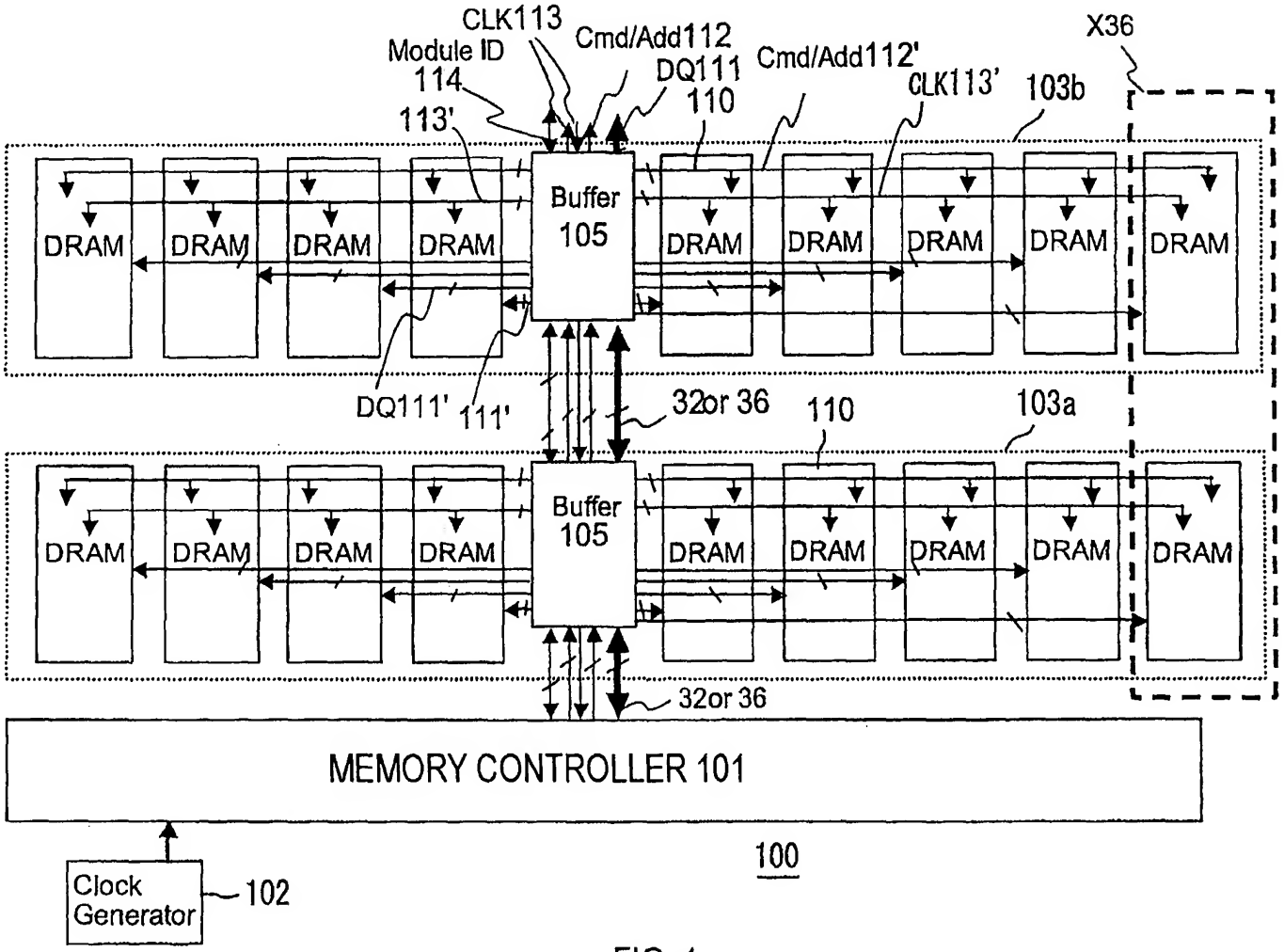

CLK113
Module ID
114
Cmd/Add112
DQ111
110
Cmd/Add112'
CLK113'
X36
103b
113'
Buffer
105
DRAM
DRAM
DRAM
DRAM
DRAM
DRAM
DRAM
DRAM
DRAM
DQ111'
111'
32or 36
110
103a
Buffer
105
DRAM
DRAM
DRAM
DRAM
DRAM
DRAM
DRAM
DRAM
DRAM
32or 36
MEMORY CONTROLLER 101
100
Clock
Generator
102

FIG. 1

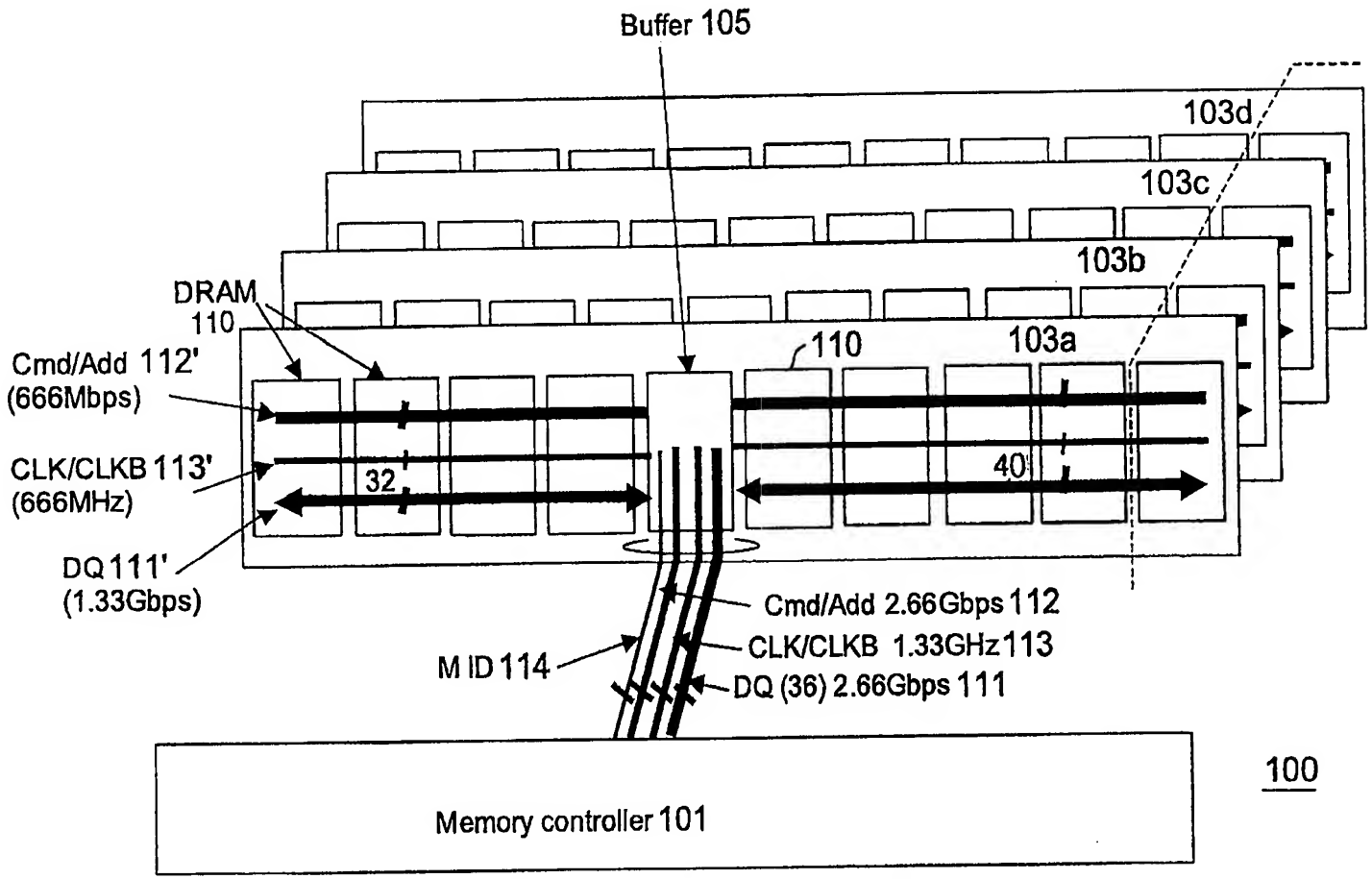

Buffer 105
103d
103c
103b
103a
DRAM
110
110
Cmd/Add 112'
(666Mbps)
CLK/CLKB 113'
(666MHz)
DQ 111'
(1.33Gbps)
32
40
Cmd/Add 2.66Gbps 112
CLK/CLKB 1.33GHz 113
DQ (36) 2.66Gbps 111
M ID 114
Memory controller 101
100

FIG. 2

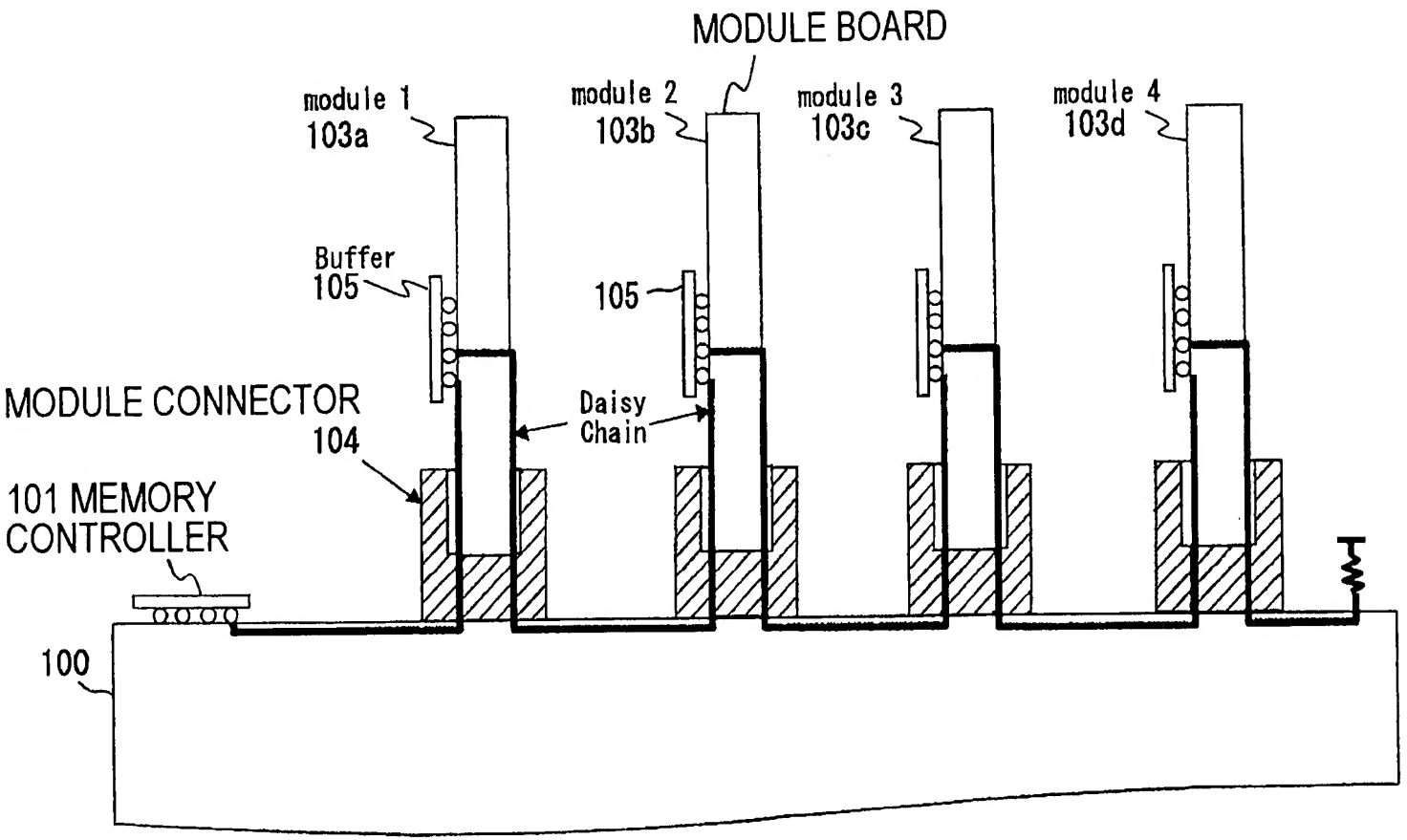

MODULE BOARD
module 1
103a
module 2
103b
module 3
103c
module 4
103d
Buffer
105
105
MODULE CONNECTOR
104
Daisy
Chain
101 MEMORY
CONTROLLER
100

FIG. 3

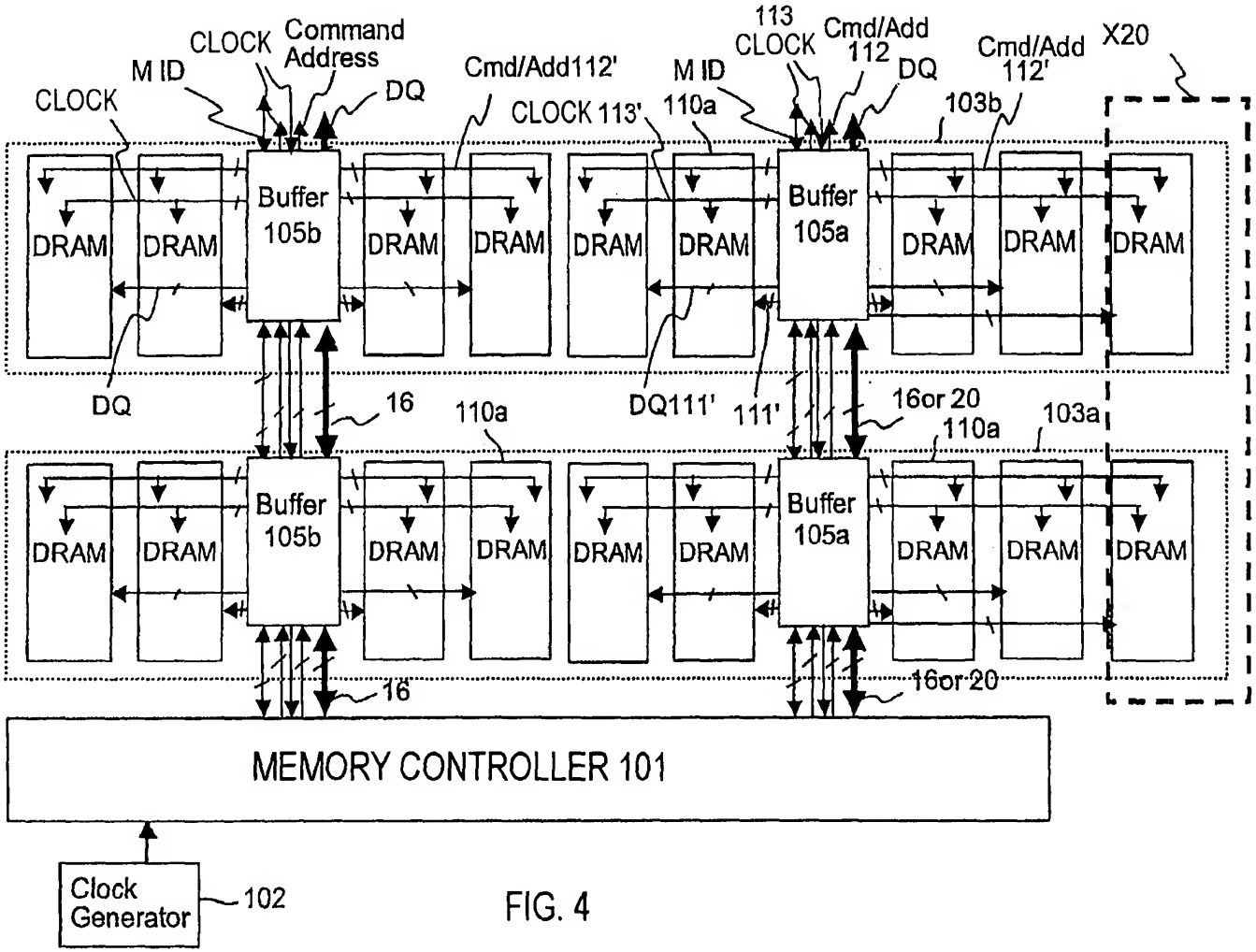

CLOCK
M ID
CLOCK
Command
Address
DQ
Cmd/Add112'
CLOCK 113'
M ID
110a
113
CLOCK
Cmd/Add
112
DQ
Cmd/Add
112'
X20
103b
Buffer
105b
Buffer
105a
DRAM
DQ
16
110a
DQ111'
111'
16or 20
110a
103a
MEMORY CONTROLLER 101
Clock
Generator
102

FIG. 4

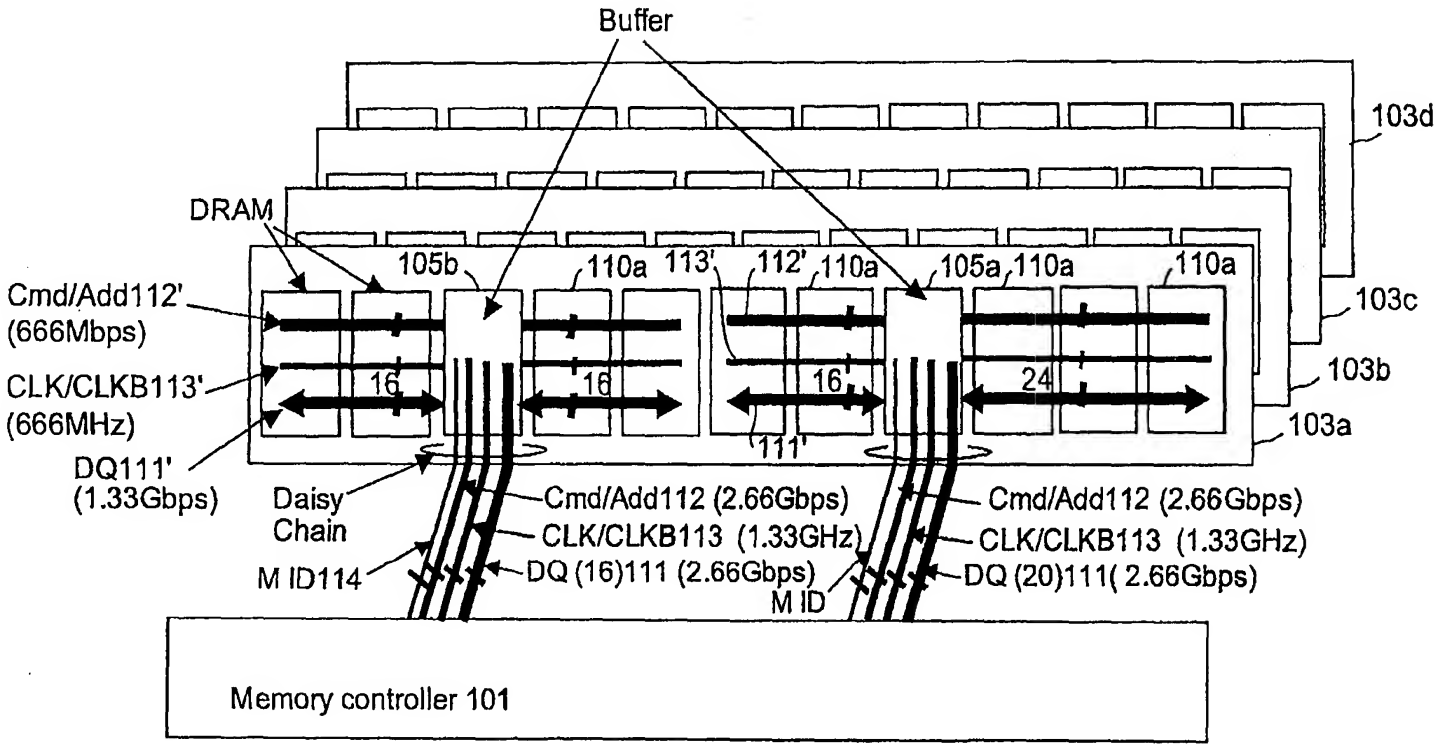

Buffer
103d
DRAM
105b
110a
113'
112'
110a
105a
110a
110a
Cmd/Add112'
(666Mbps)
CLK/CLKB113'
(666MHz)
DQ111'
(1.33Gbps)
16
16
16
24
103c
103b
103a
111'
Daisy
Chain
Cmd/Add112 (2.66Gbps)
CLK/CLKB113 (1.33GHz)
DQ (16)111 (2.66Gbps)
M ID114
Cmd/Add112 (2.66Gbps)
CLK/CLKB113 (1.33GHz)
DQ (20)111(2.66Gbps)
M ID
Memory controller 101

FIG. 5

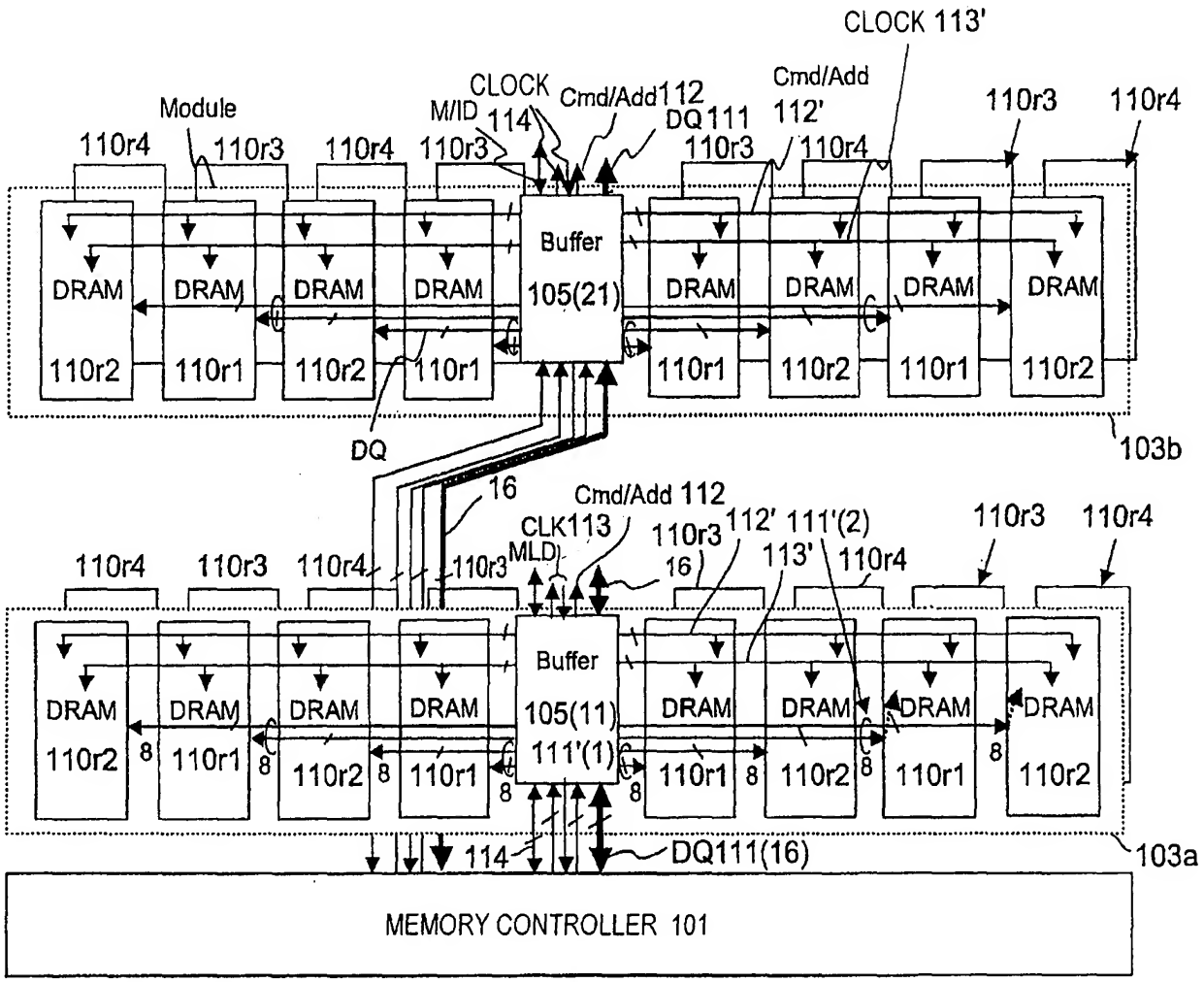

CLOCK 113'
Module
CLOCK
M/ID 114
Cmd/Add 112
DQ 111
Cmd/Add
112'
110r3
110r4
Buffer
105(21)
DRAM
110r2
110r1
103b
DQ
16
Cmd/Add 112
CLK113
MLD
112'
111'(2)
113'
Buffer
105(11)
111'(1)
8
114
DQ111(16)
103a
MEMORY CONTROLLER 101

FIG. 6

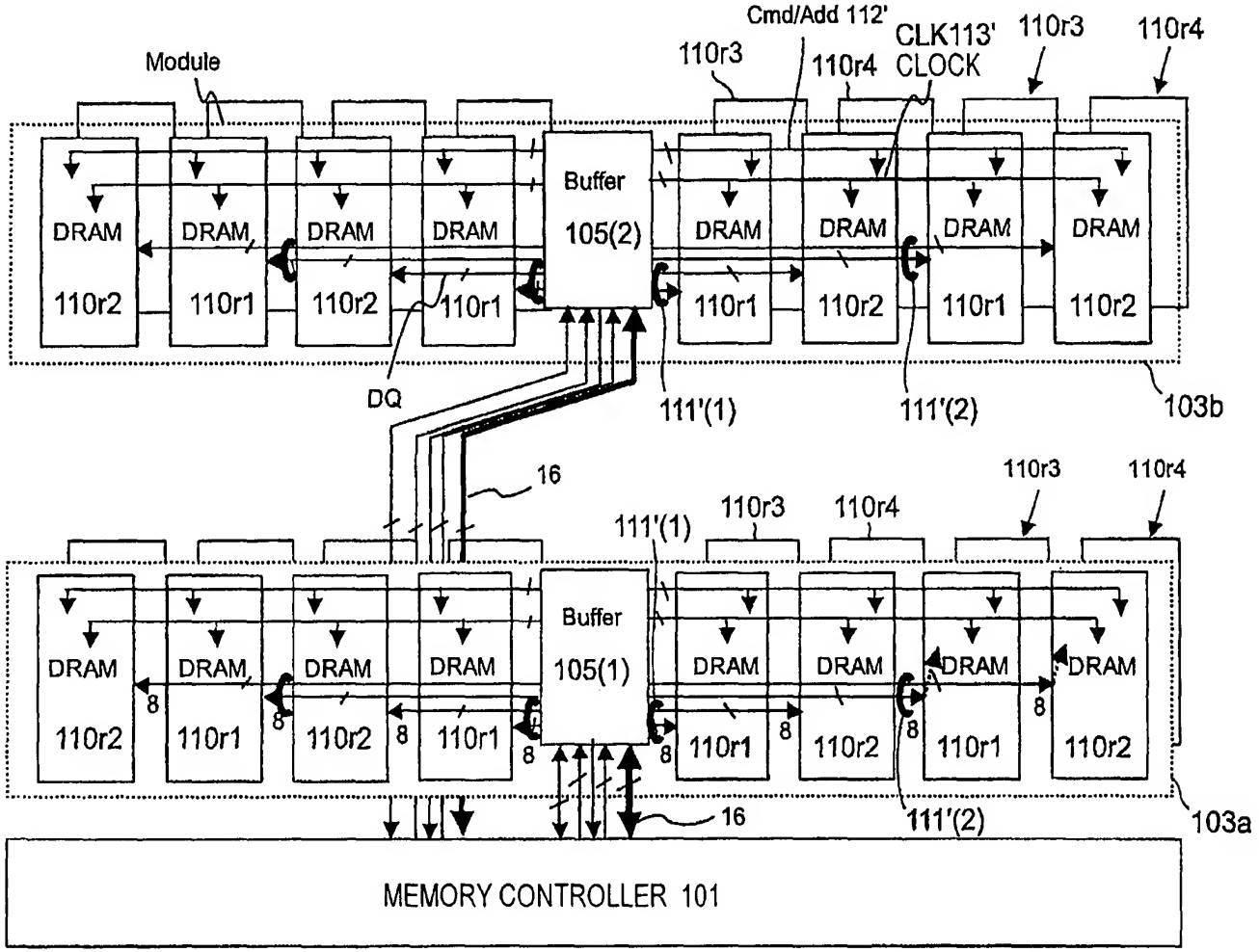

Module
Cmd/Add 112'
CLK113'
CLOCK
110r3
110r4
110r3
110r4
Buffer
105(2)
DRAM
110r2
110r1
DQ
111'(1)
111'(2)
103b
16
Buffer
105(1)
8
16
MEMORY CONTROLLER 101
103a

FIG. 7

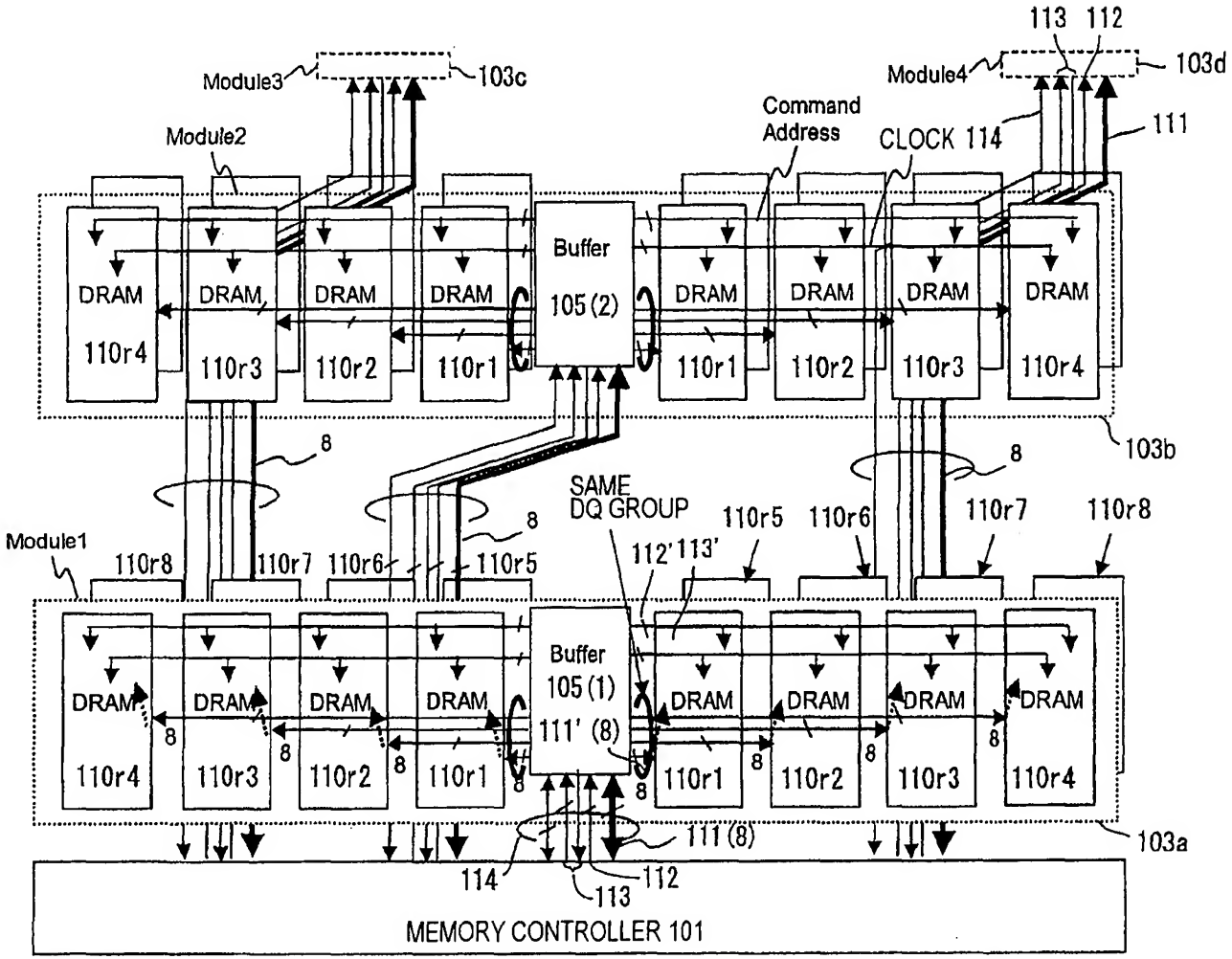

113 112
Module3
103c
Module4
103d
Command
Address
CLOCK 114
111
Module2
Buffer
105 (2)
DRAM
110r4
110r3
110r2
110r1
103b
8
SAME
DQ GROUP
110r5
110r6
110r7
110r8
Module1
112' 113'
Buffer
105 (1)
111' (8)
111 (8)
103a
114
113
112
MEMORY CONTROLLER 101

FIG. 8

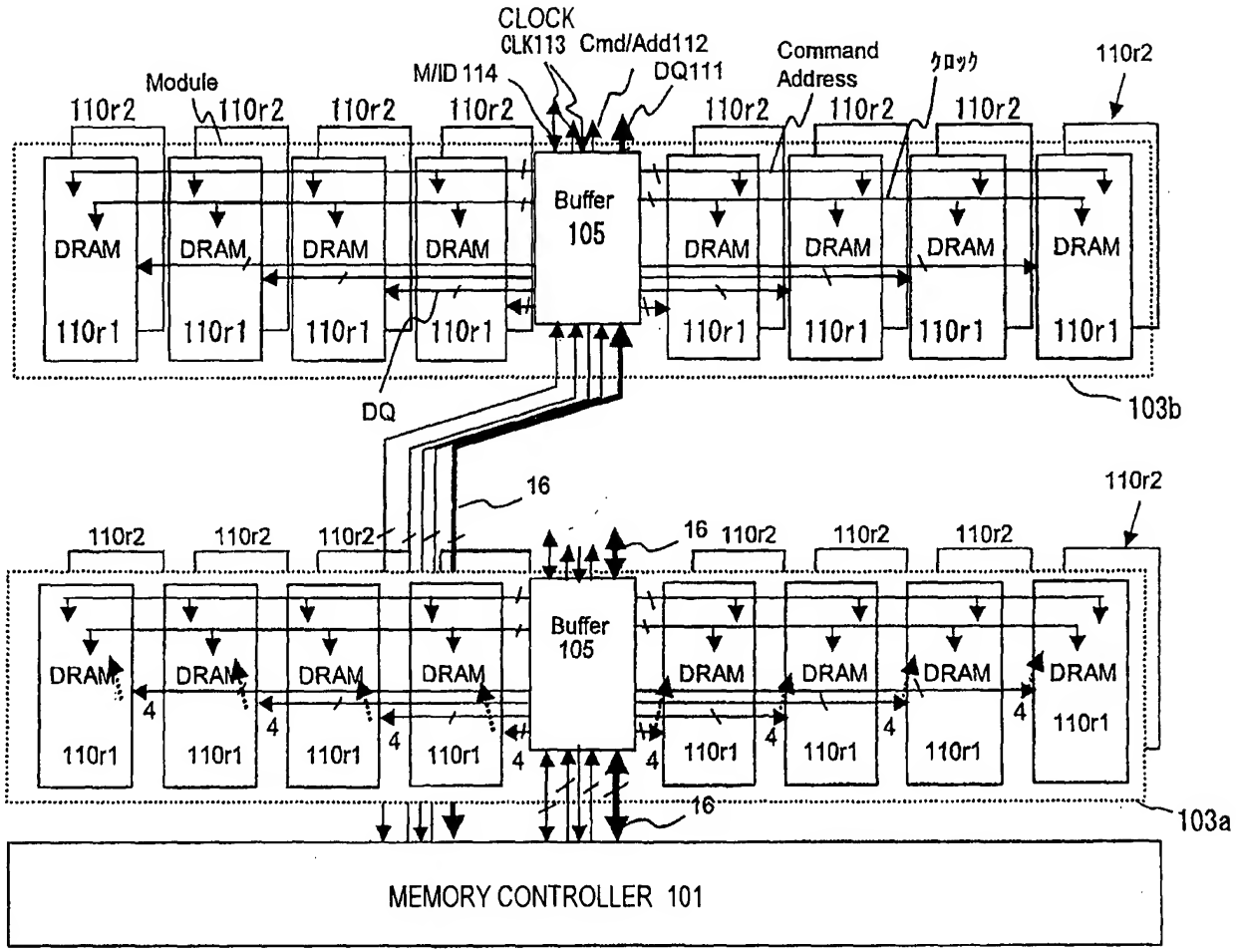

CLOCK
CLK113
Cmd/Add112
M/ID 114
DQ111
Command
Address
クロック
Module
110r2
DRAM
110r1
Buffer
105
DQ
16
103b
103a
MEMORY CONTROLLER 101

FIG. 9

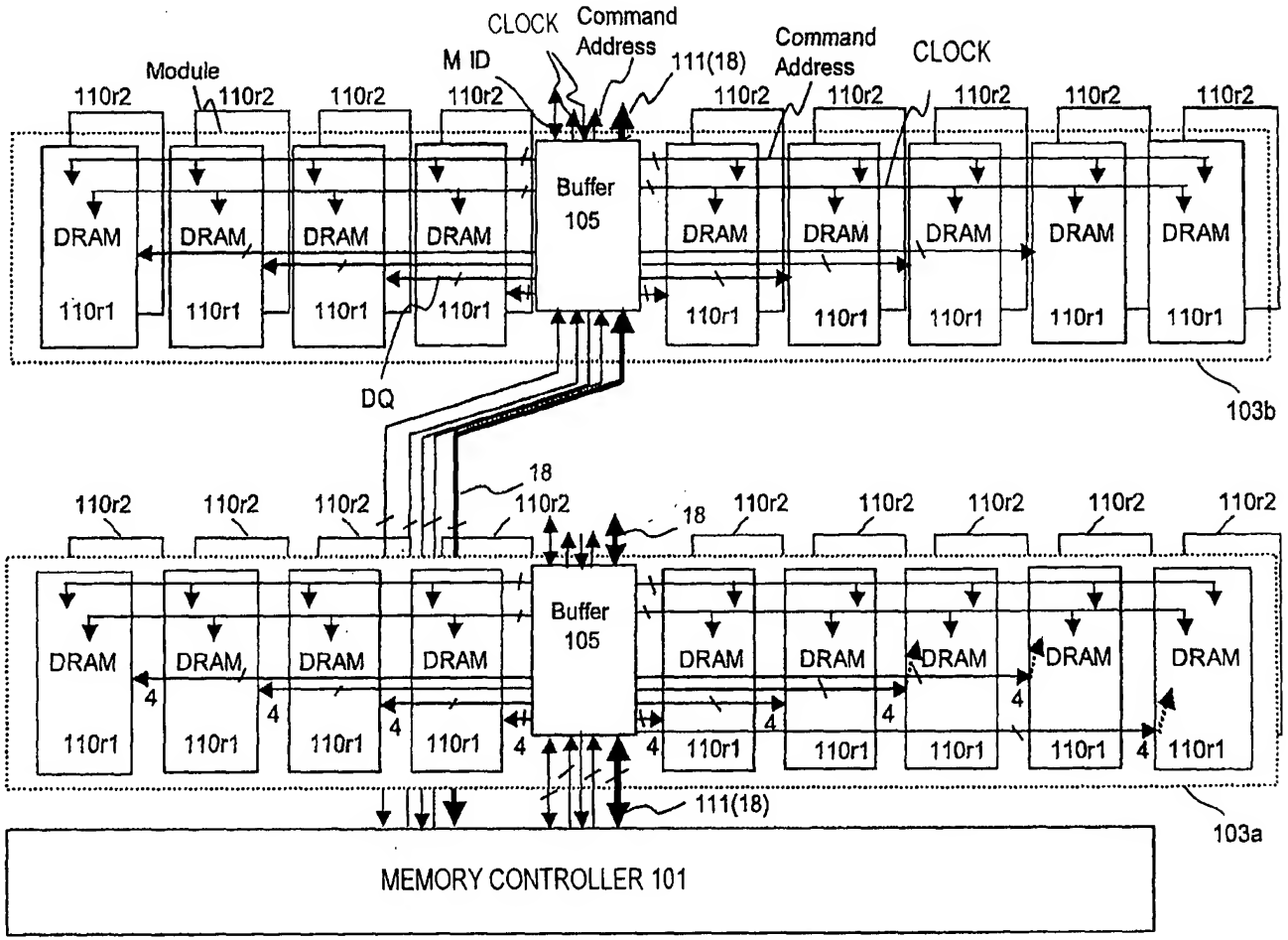

CLOCK
Command
Address
M ID
111(18)
Command
Address
CLOCK
Module
110r2
Buffer
105
DRAM
110r1
DQ
103b
18
Buffer
105
4
111(18)
103a
MEMORY CONTROLLER 101

FIG. 10

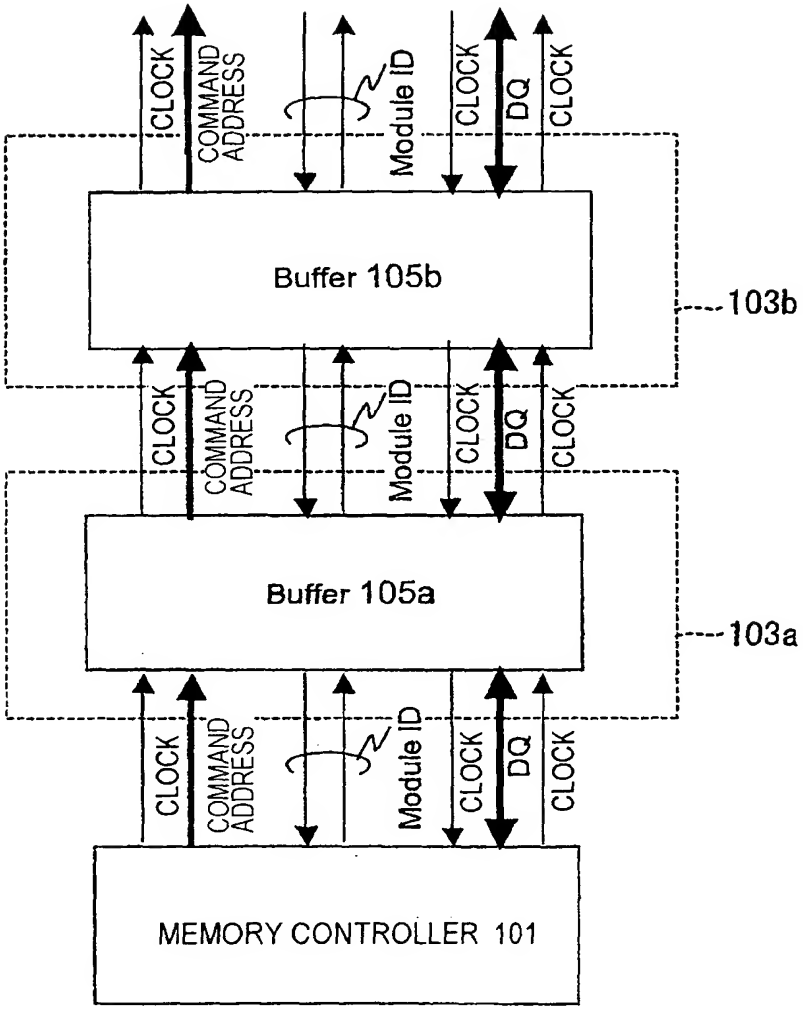

CLOCK
COMMAND ADDRESS
Module ID
CLOCK
DQ
CLOCK
Buffer 105b
103b
CLOCK
COMMAND ADDRESS
Module ID
CLOCK
DQ
CLOCK
Buffer 105a
103a
CLOCK
COMMAND ADDRESS
Module ID
CLOCK
DQ
CLOCK
MEMORY CONTROLLER 101

FIG. 11

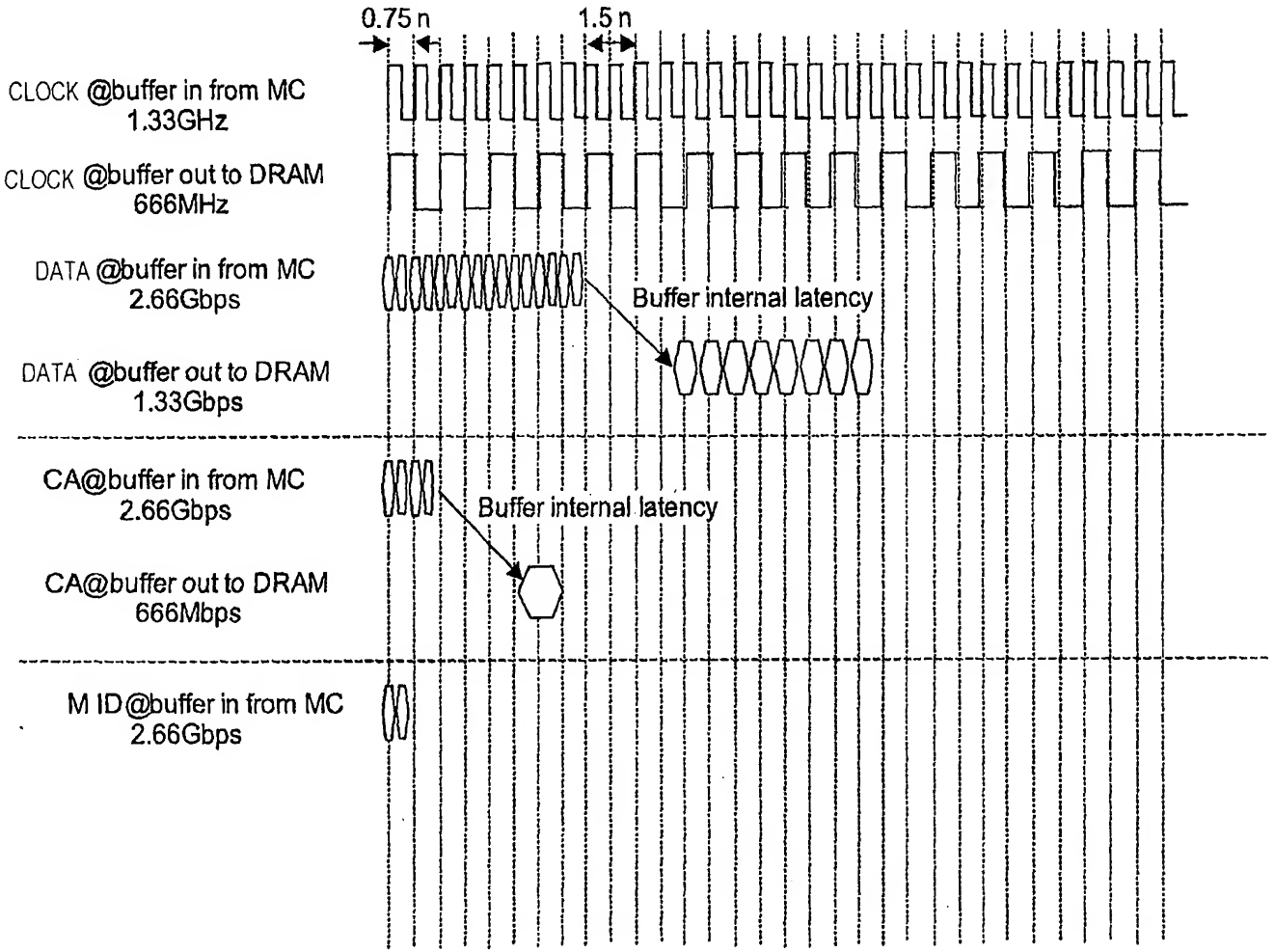

0.75 n
1.5 n
CLOCK @buffer in from MC
1.33GHz
CLOCK @buffer out to DRAM
666MHz
DATA @buffer in from MC
2.66Gbps
Buffer internal latency
DATA @buffer out to DRAM
1.33Gbps
CA@buffer in from MC
2.66Gbps
Buffer internal latency
CA@buffer out to DRAM
666Mbps
M ID@buffer in from MC
2.66Gbps

FIG. 12

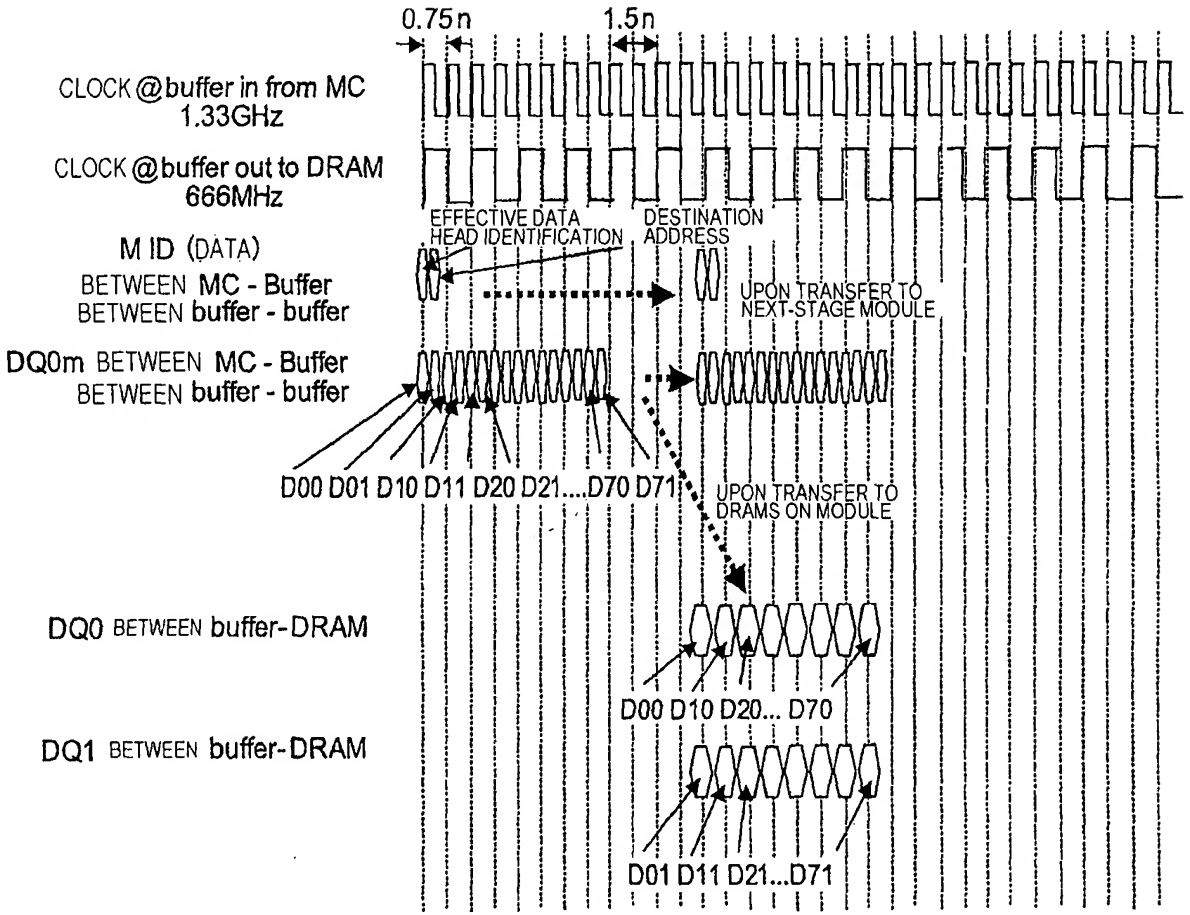

0.75n
1.5n
CLOCK @buffer in from MC
1.33GHz
CLOCK @buffer out to DRAM
666MHz
EFFECTIVE DATA
HEAD IDENTIFICATION
DESTINATION
ADDRESS
M ID (DATA)
BETWEEN MC - Buffer
BETWEEN buffer - buffer
UPON TRANSFER TO
NEXT-STAGE MODULE
DQ0m BETWEEN MC - Buffer
BETWEEN buffer - buffer
D00 D01 D10 D11 D20 D21....D70 D71
UPON TRANSFER TO
DRAMS ON MODULE
DQ0 BETWEEN buffer-DRAM
D00 D10 D20... D70
DQ1 BETWEEN buffer-DRAM
D01 D11 D21...D71

FIG. 13

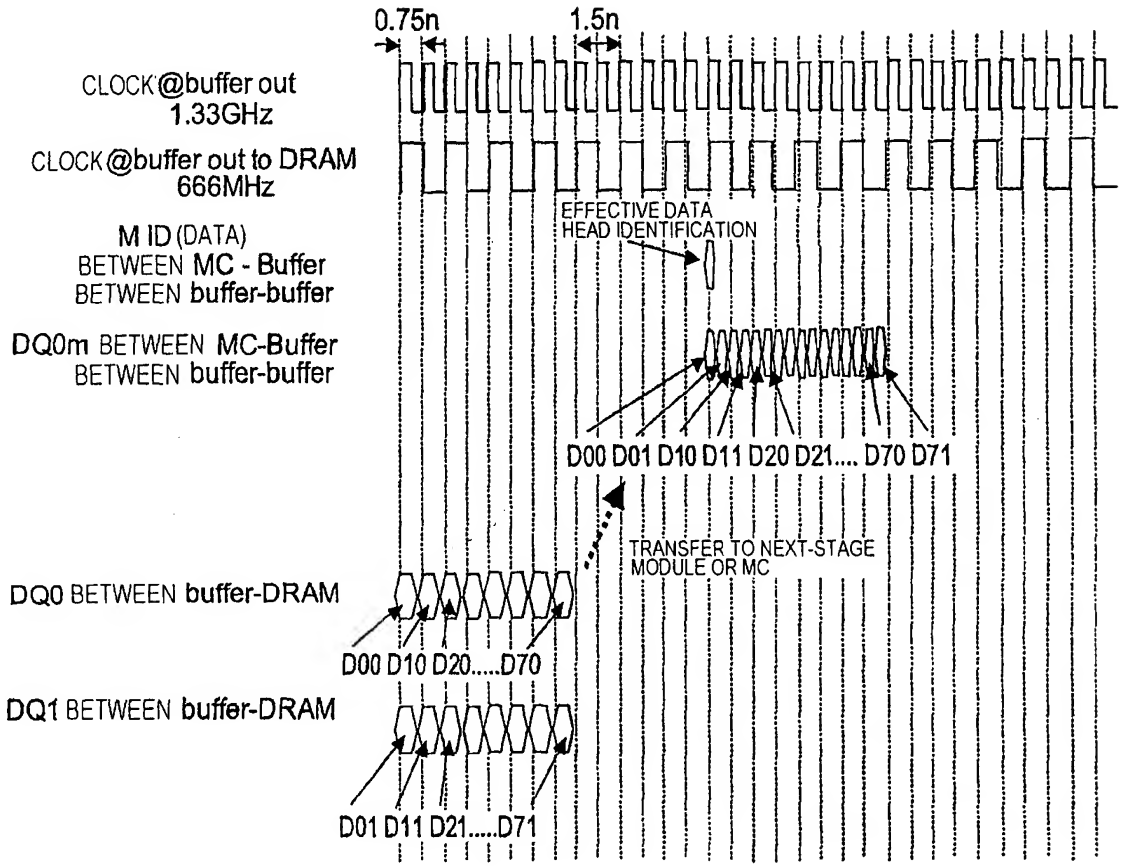

0.75n
1.5n
CLOCK@buffer out
1.33GHz
CLOCK@buffer out to DRAM
666MHz
M ID (DATA)
BETWEEN MC - Buffer
BETWEEN buffer-buffer
DQ0m BETWEEN MC-Buffer
BETWEEN buffer-buffer
EFFECTIVE DATA
HEAD IDENTIFICATION
D00 D01 D10 D11 D20 D21.... D70 D71
TRANSFER TO NEXT-STAGE
MODULE OR MC
DQ0 BETWEEN buffer-DRAM
D00 D10 D20.....D70
DQ1 BETWEEN buffer-DRAM
D01 D11 D21.....D71

FIG. 14

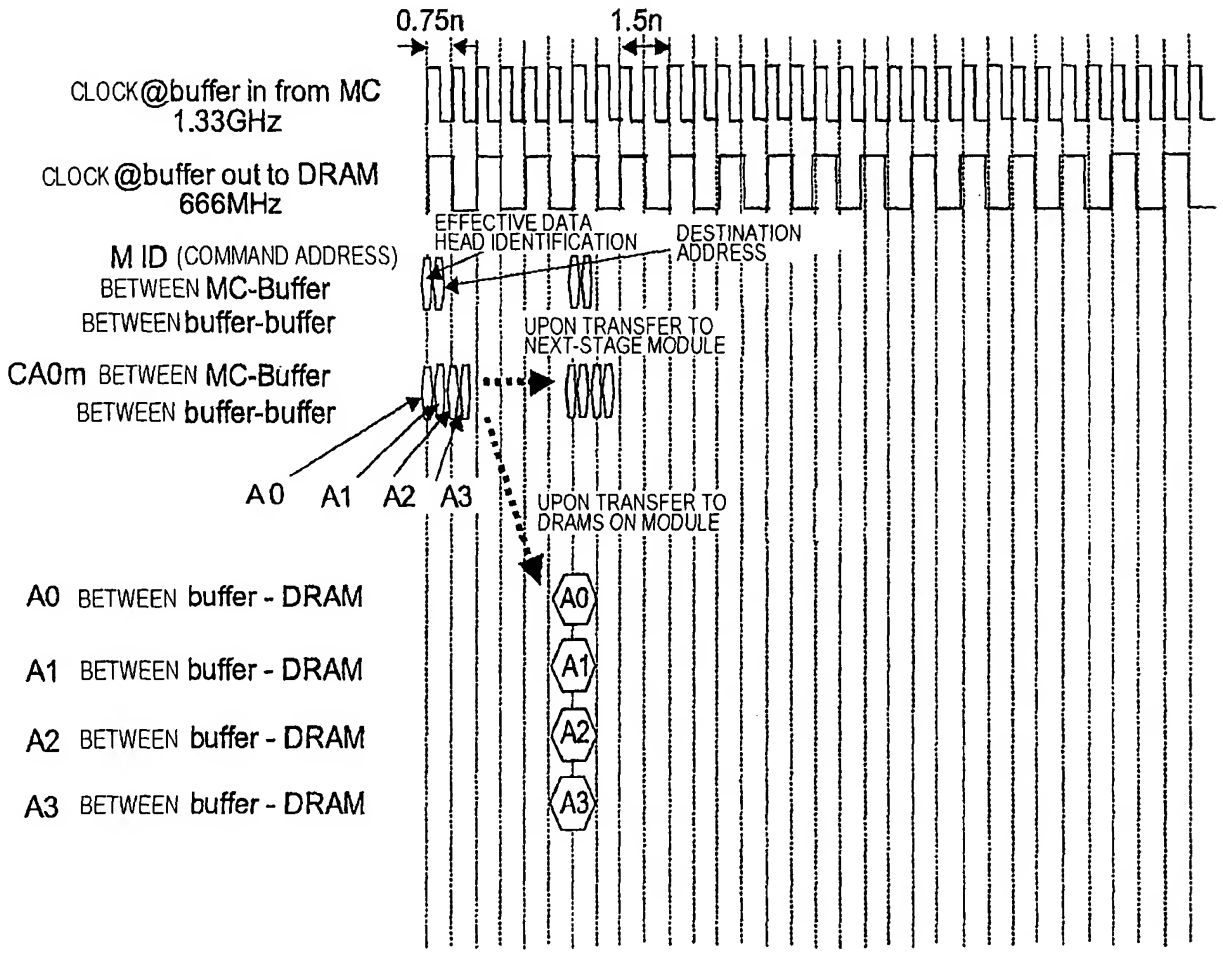

0.75n
1.5n
CLOCK@buffer in from MC
1.33GHz
CLOCK @buffer out to DRAM
666MHz
EFFECTIVE DATA
HEAD IDENTIFICATION
DESTINATION
ADDRESS
M ID (COMMAND ADDRESS)
BETWEEN MC-Buffer
BETWEEN buffer-buffer
UPON TRANSFER TO
NEXT-STAGE MODULE
CA0m BETWEEN MC-Buffer
BETWEEN buffer-buffer
A0
A1
A2
A3
UPON TRANSFER TO
DRAMS ON MODULE
A0 BETWEEN buffer - DRAM
A1 BETWEEN buffer - DRAM
A2 BETWEEN buffer - DRAM
A3 BETWEEN buffer - DRAM
A0
A1
A2
A3

FIG. 15

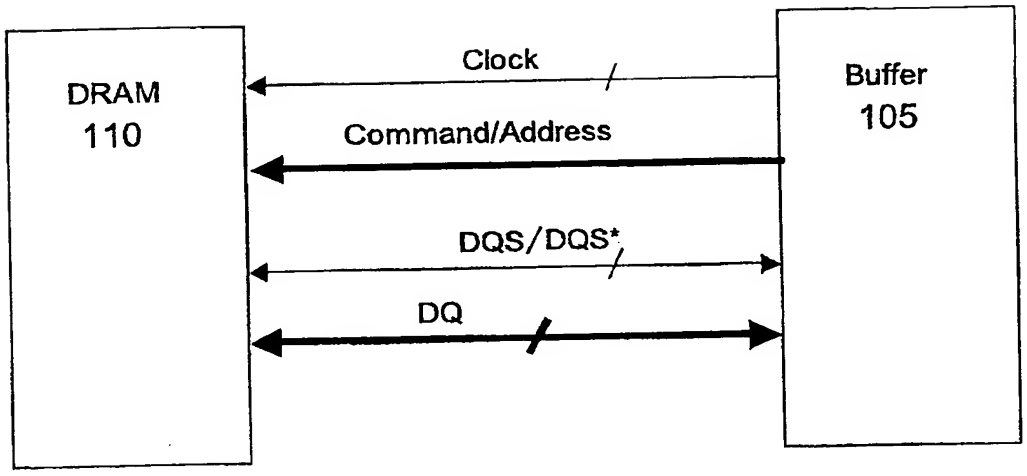


FIG. 16

FIG. 17A

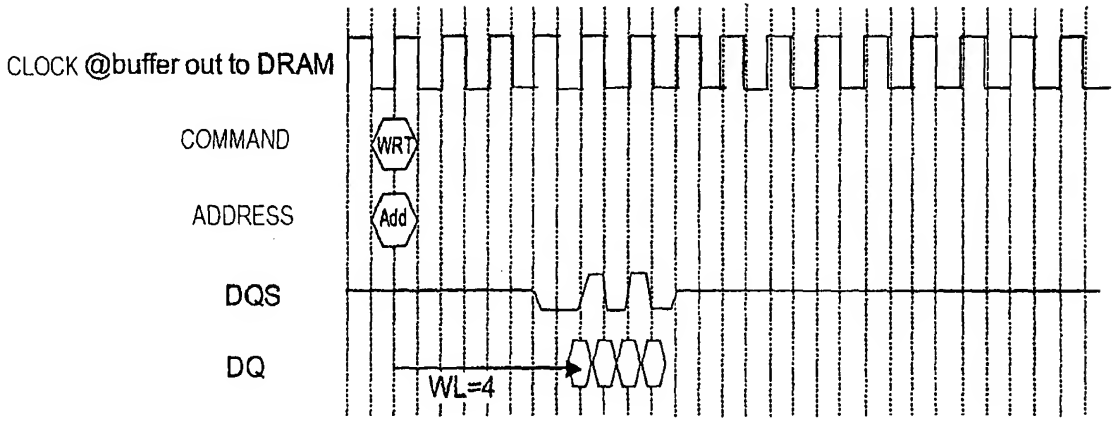
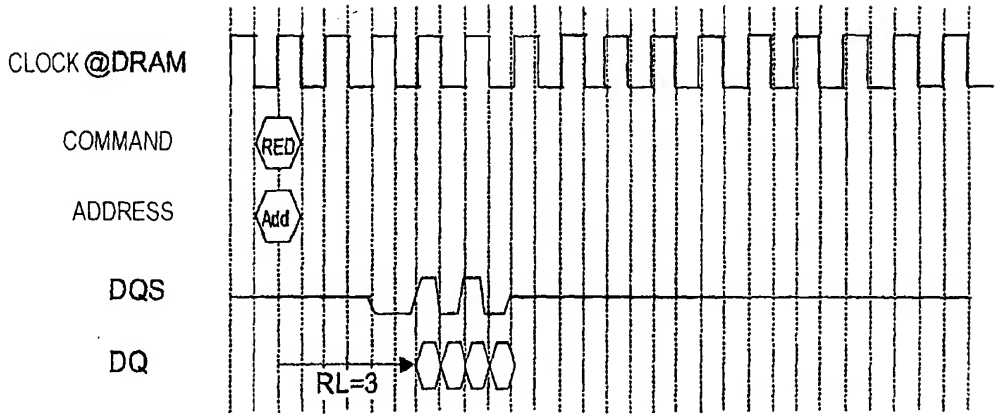


FIG. 17B



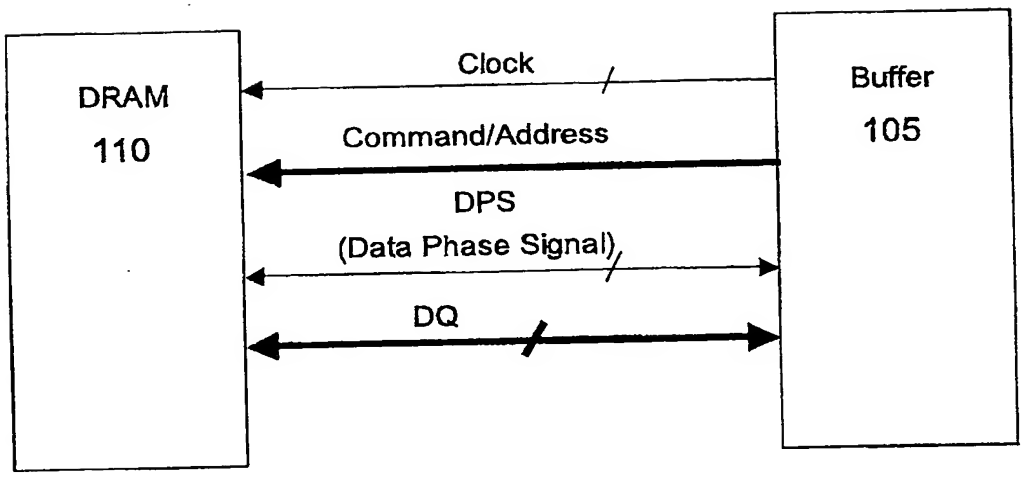

DRAM
110
Clock
Command/Address
DPS
(Data Phase Signal)
DQ
Buffer
105

FIG. 18

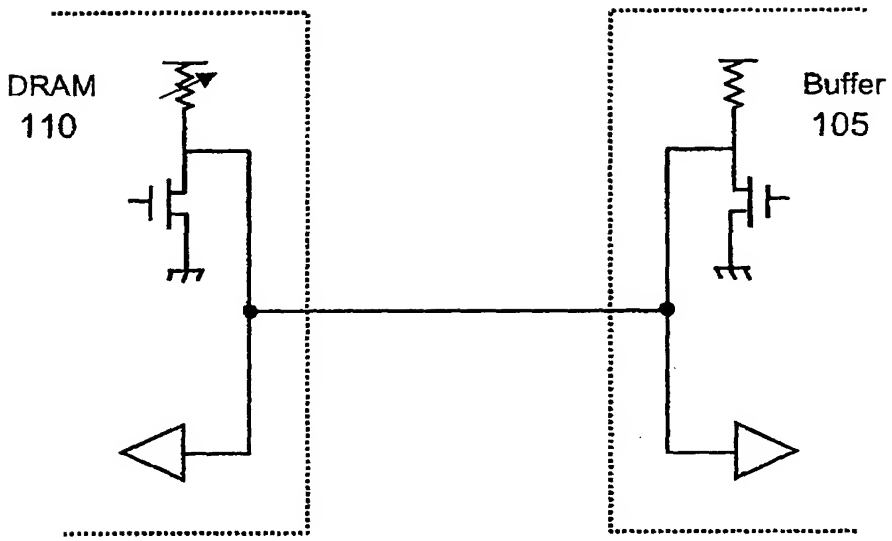


FIG. 19

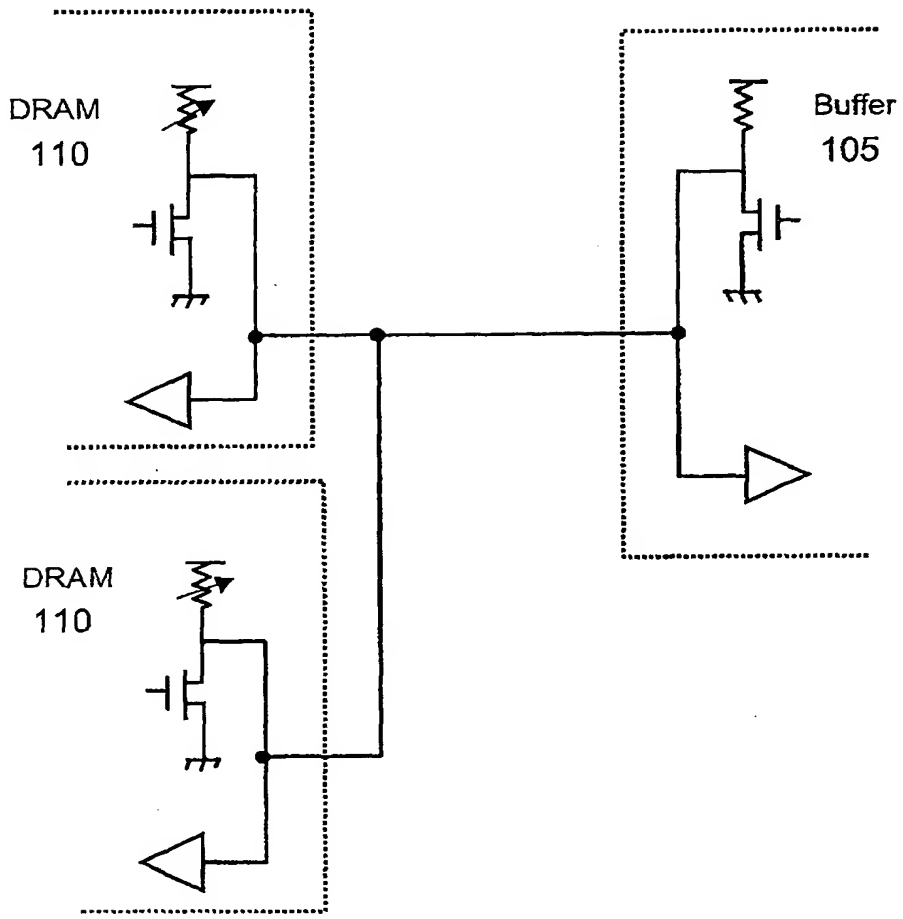


FIG. 20

FIG. 21A

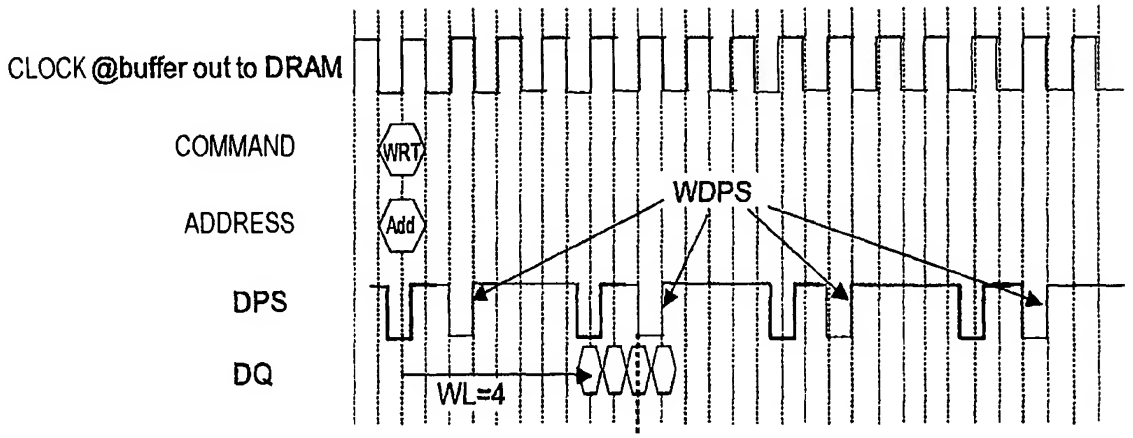
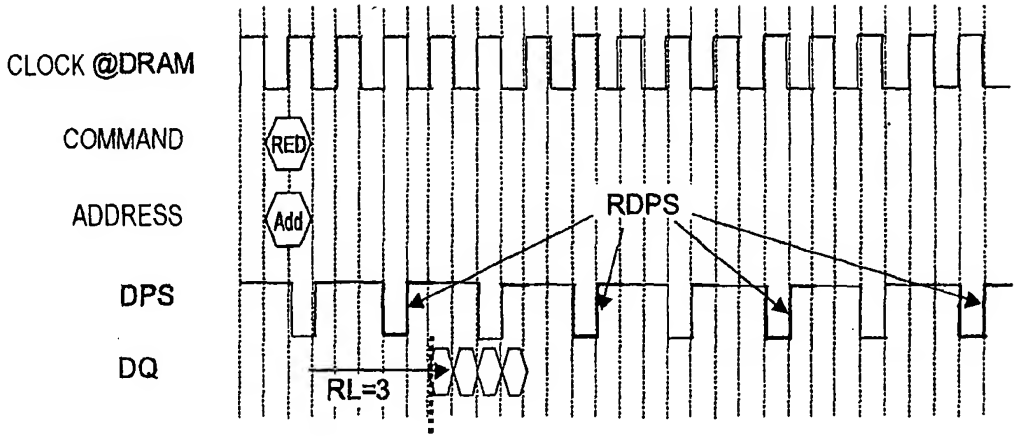


FIG. 21B



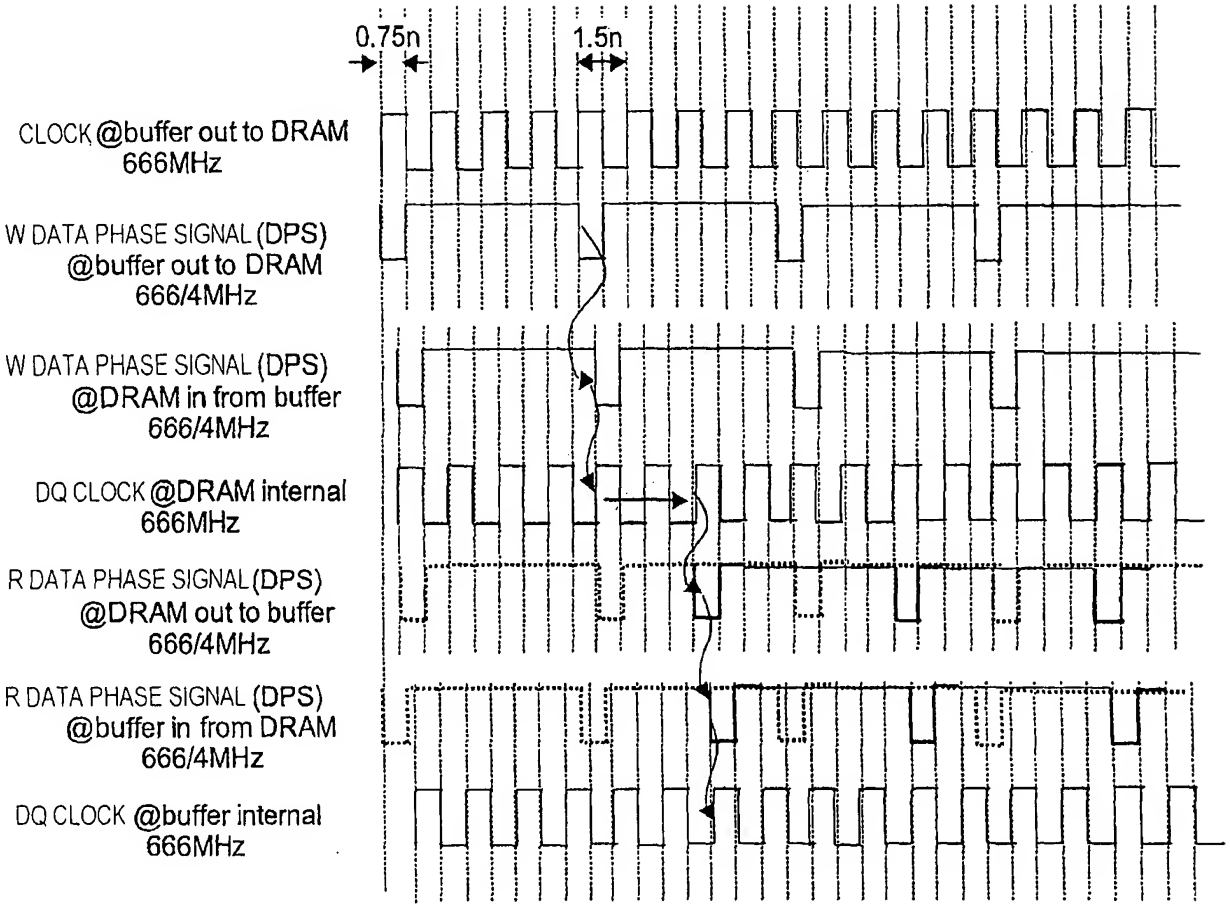

0.75n
1.5n
CLOCK @buffer out to DRAM 666MHz
W DATA PHASE SIGNAL (DPS) @buffer out to DRAM 666/4MHz
W DATA PHASE SIGNAL (DPS) @DRAM in from buffer 666/4MHz
DQ CLOCK @DRAM internal 666MHz
R DATA PHASE SIGNAL (DPS) @DRAM out to buffer 666/4MHz
R DATA PHASE SIGNAL (DPS) @buffer in from DRAM 666/4MHz
DQ CLOCK @buffer internal 666MHz

FIG. 22

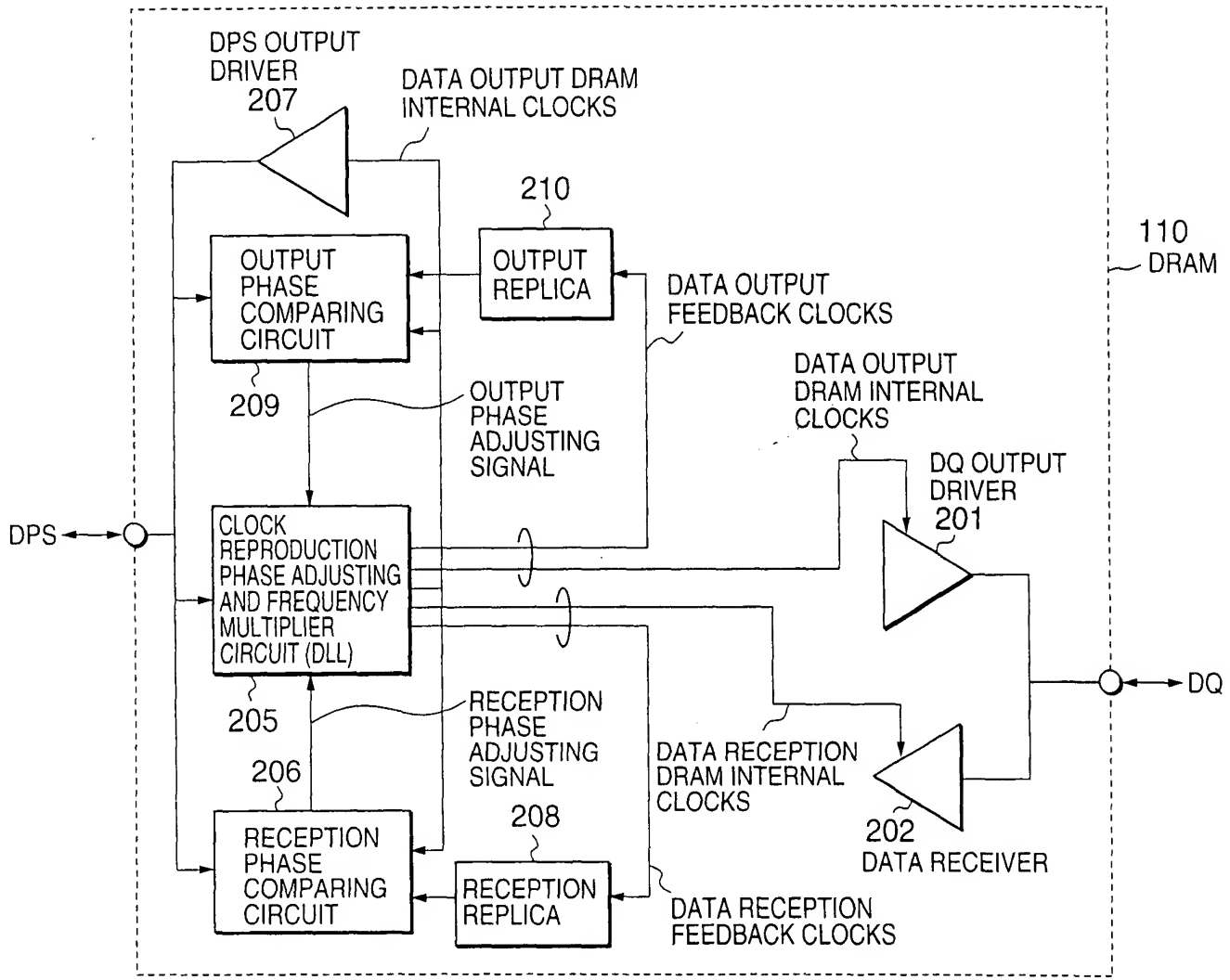

DPS OUTPUT DRIVER
207
DATA OUTPUT DRAM INTERNAL CLOCKS
210
OUTPUT REPLICA
110
DRAM
OUTPUT PHASE COMPARING CIRCUIT
DATA OUTPUT FEEDBACK CLOCKS
209
OUTPUT PHASE ADJUSTING SIGNAL
DATA OUTPUT DRAM INTERNAL CLOCKS
DQ OUTPUT DRIVER
201
DPS
CLOCK REPRODUCTION PHASE ADJUSTING AND FREQUENCY MULTIPLIER CIRCUIT (DLL)
DQ
205
RECEPTION PHASE ADJUSTING SIGNAL
206
DATA RECEPTION DRAM INTERNAL CLOCKS
208
202
DATA RECEIVER
RECEPTION PHASE COMPARING CIRCUIT
RECEPTION REPLICA
DATA RECEPTION FEEDBACK CLOCKS

FIG.23

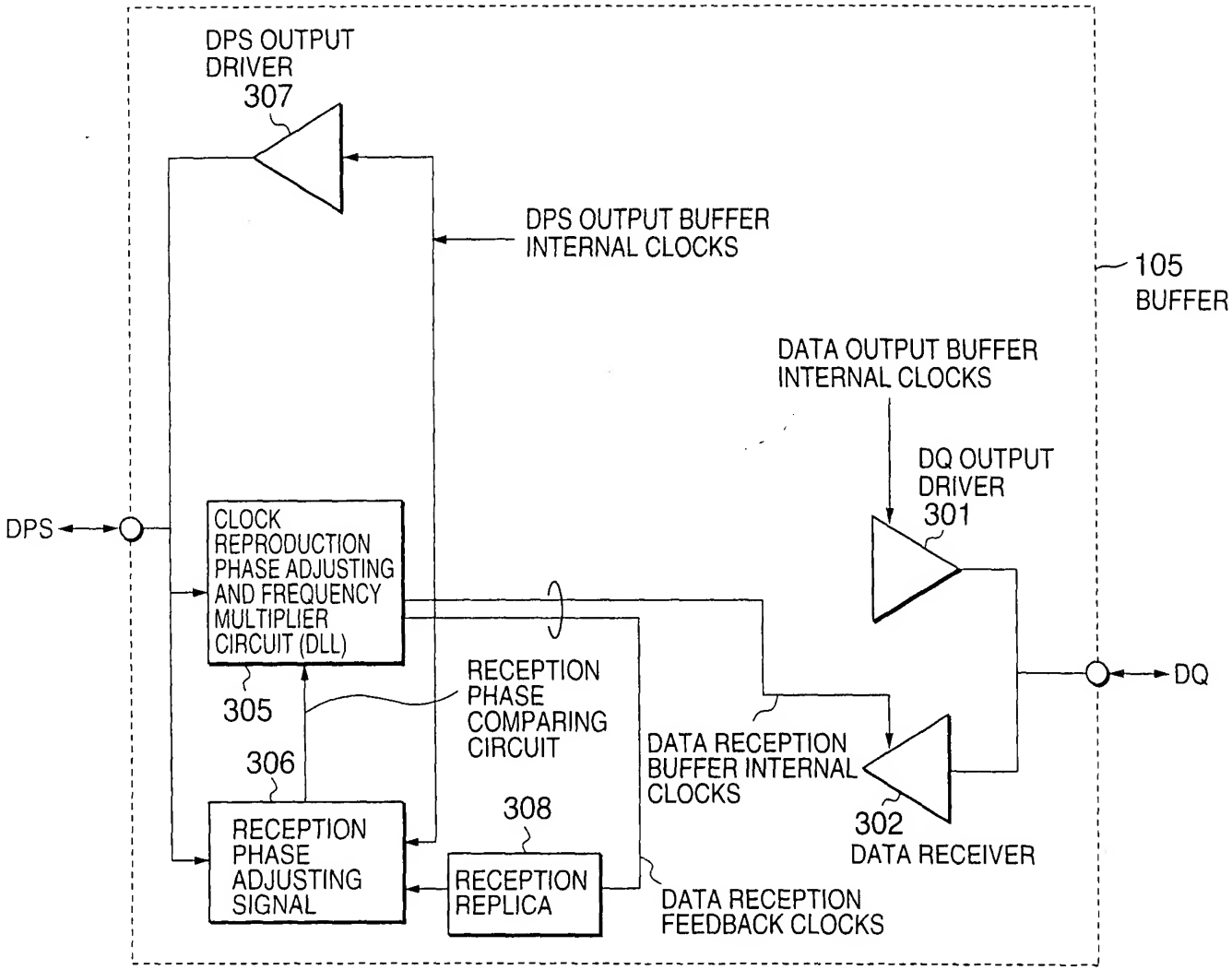

DPS OUTPUT
DRIVER
307
DPS OUTPUT BUFFER
INTERNAL CLOCKS
105
BUFFER
DATA OUTPUT BUFFER
INTERNAL CLOCKS
DQ OUTPUT
DRIVER
301
DPS
CLOCK
REPRODUCTION
PHASE ADJUSTING
AND FREQUENCY
MULTIPLIER
CIRCUIT (DLL)
305
RECEPTION
PHASE
COMPARING
CIRCUIT
306
308
RECEPTION
PHASE
ADJUSTING
SIGNAL
RECEPTION
REPLICA
DATA RECEPTION
BUFFER INTERNAL
CLOCKS
302
DATA RECEIVER
DQ
DATA RECEPTION
FEEDBACK CLOCKS

FIG.24

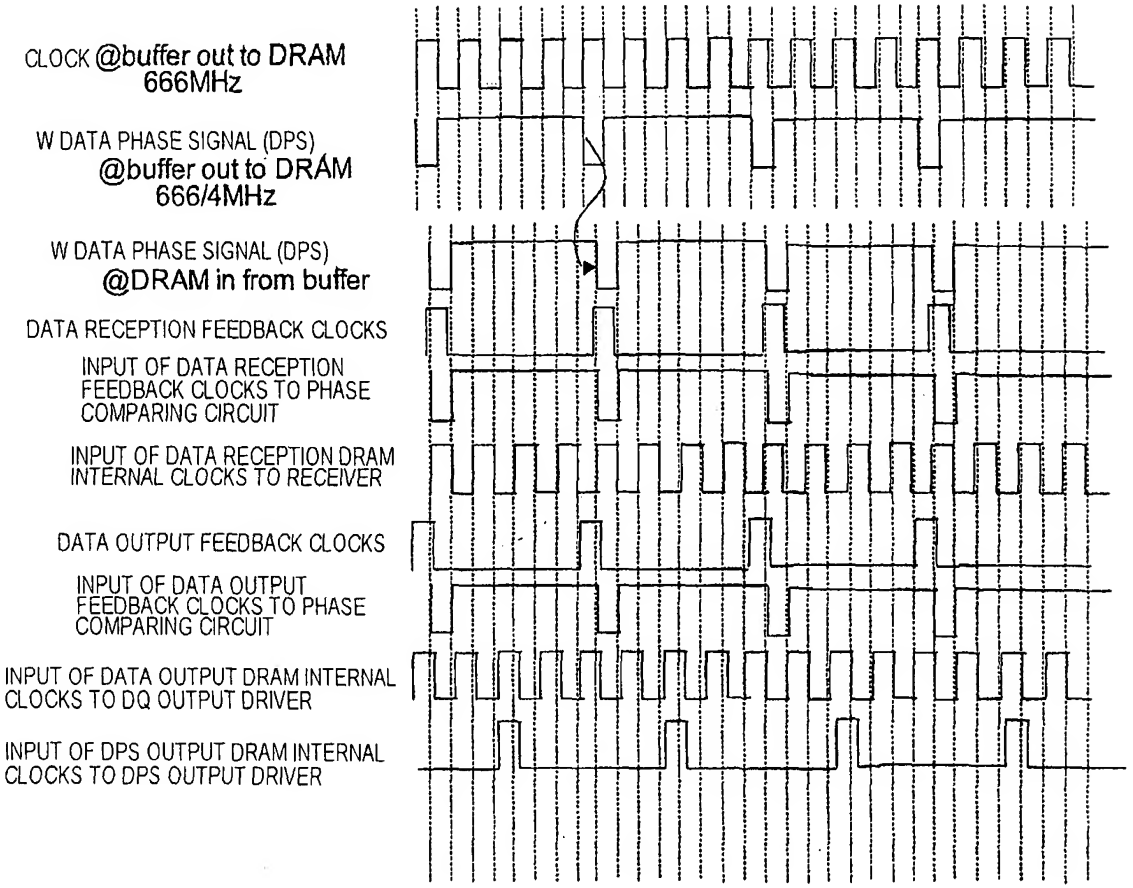

CLOCK @buffer out to DRAM 666MHz
W DATA PHASE SIGNAL (DPS) @buffer out to DRAM 666/4MHz
W DATA PHASE SIGNAL (DPS) @DRAM in from buffer
DATA RECEPTION FEEDBACK CLOCKS
INPUT OF DATA RECEPTION FEEDBACK CLOCKS TO PHASE COMPARING CIRCUIT
INPUT OF DATA RECEPTION DRAM INTERNAL CLOCKS TO RECEIVER
DATA OUTPUT FEEDBACK CLOCKS
INPUT OF DATA OUTPUT FEEDBACK CLOCKS TO PHASE COMPARING CIRCUIT
INPUT OF DATA OUTPUT DRAM INTERNAL CLOCKS TO DQ OUTPUT DRIVER
INPUT OF DPS OUTPUT DRAM INTERNAL CLOCKS TO DPS OUTPUT DRIVER

FIG. 25

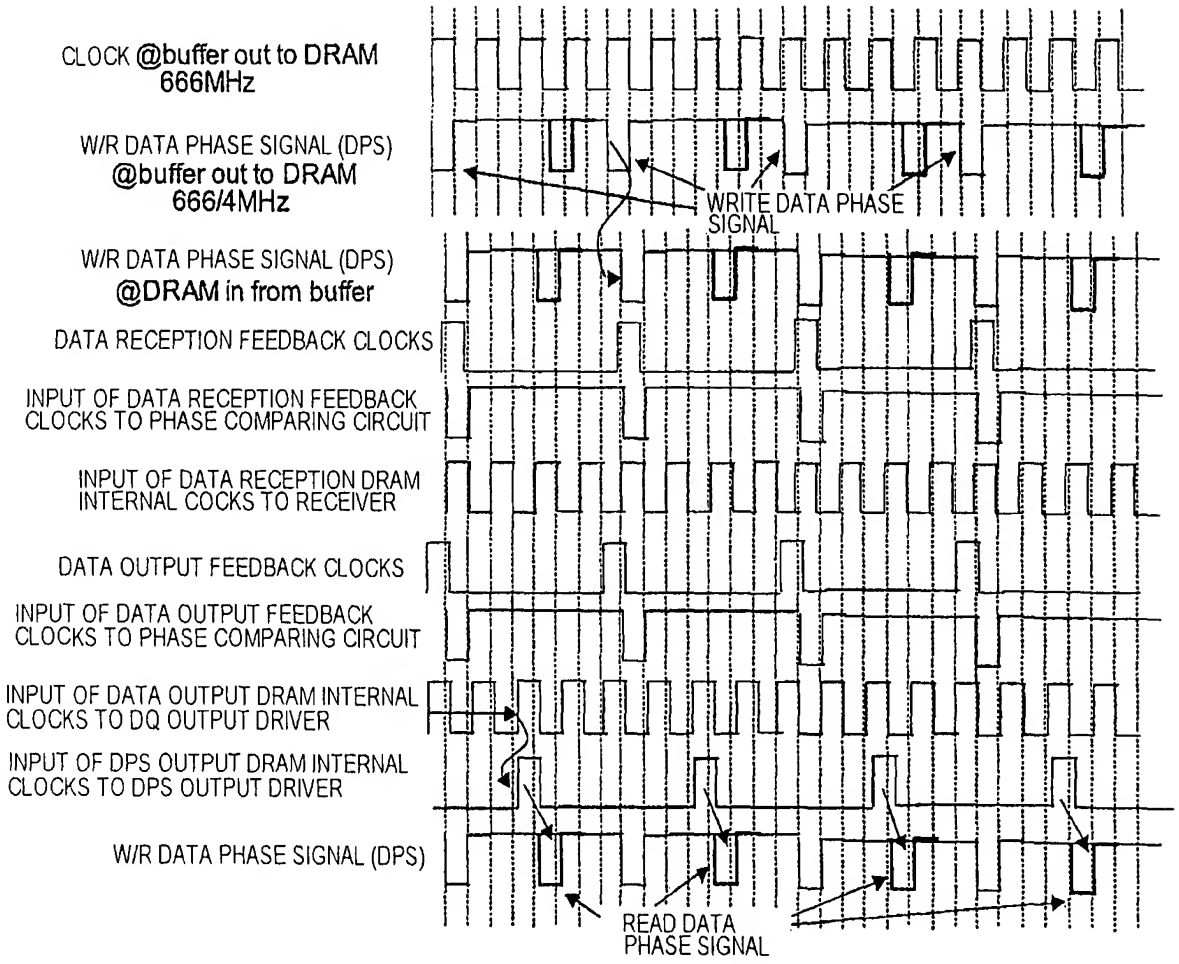

CLOCK @buffer out to DRAM 666MHz
W/R DATA PHASE SIGNAL (DPS) @buffer out to DRAM 666/4MHz
WRITE DATA PHASE SIGNAL
W/R DATA PHASE SIGNAL (DPS) @DRAM in from buffer
DATA RECEPTION FEEDBACK CLOCKS
INPUT OF DATA RECEPTION FEEDBACK CLOCKS TO PHASE COMPARING CIRCUIT
INPUT OF DATA RECEPTION DRAM INTERNAL COCKS TO RECEIVER
DATA OUTPUT FEEDBACK CLOCKS
INPUT OF DATA OUTPUT FEEDBACK CLOCKS TO PHASE COMPARING CIRCUIT
INPUT OF DATA OUTPUT DRAM INTERNAL CLOCKS TO DQ OUTPUT DRIVER
INPUT OF DPS OUTPUT DRAM INTERNAL CLOCKS TO DPS OUTPUT DRIVER
W/R DATA PHASE SIGNAL (DPS)
READ DATA PHASE SIGNAL

FIG. 26

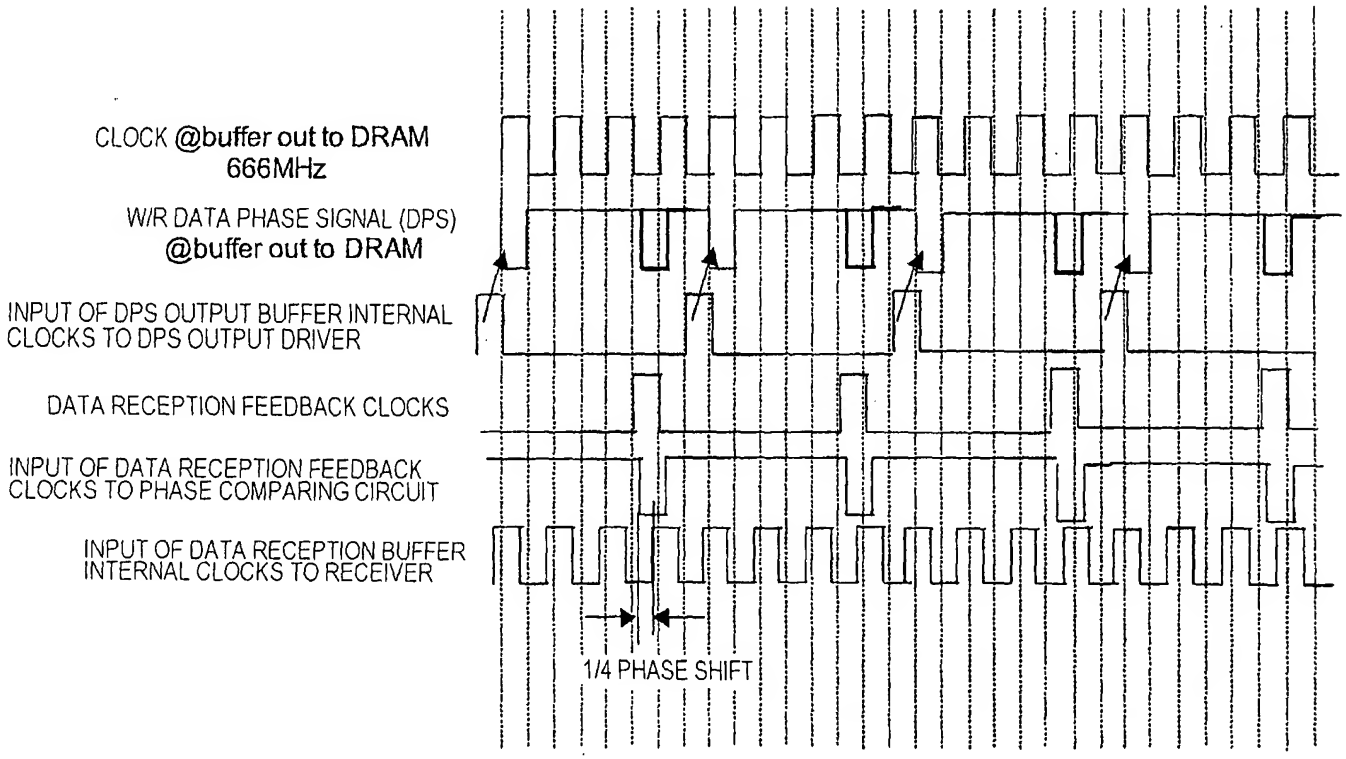

CLOCK @buffer out to DRAM
666MHz
W/R DATA PHASE SIGNAL (DPS)
@buffer out to DRAM
INPUT OF DPS OUTPUT BUFFER INTERNAL CLOCKS TO DPS OUTPUT DRIVER
DATA RECEPTION FEEDBACK CLOCKS
INPUT OF DATA RECEPTION FEEDBACK CLOCKS TO PHASE COMPARING CIRCUIT
INPUT OF DATA RECEPTION BUFFER INTERNAL CLOCKS TO RECEIVER
1/4 PHASE SHIFT

FIG. 27

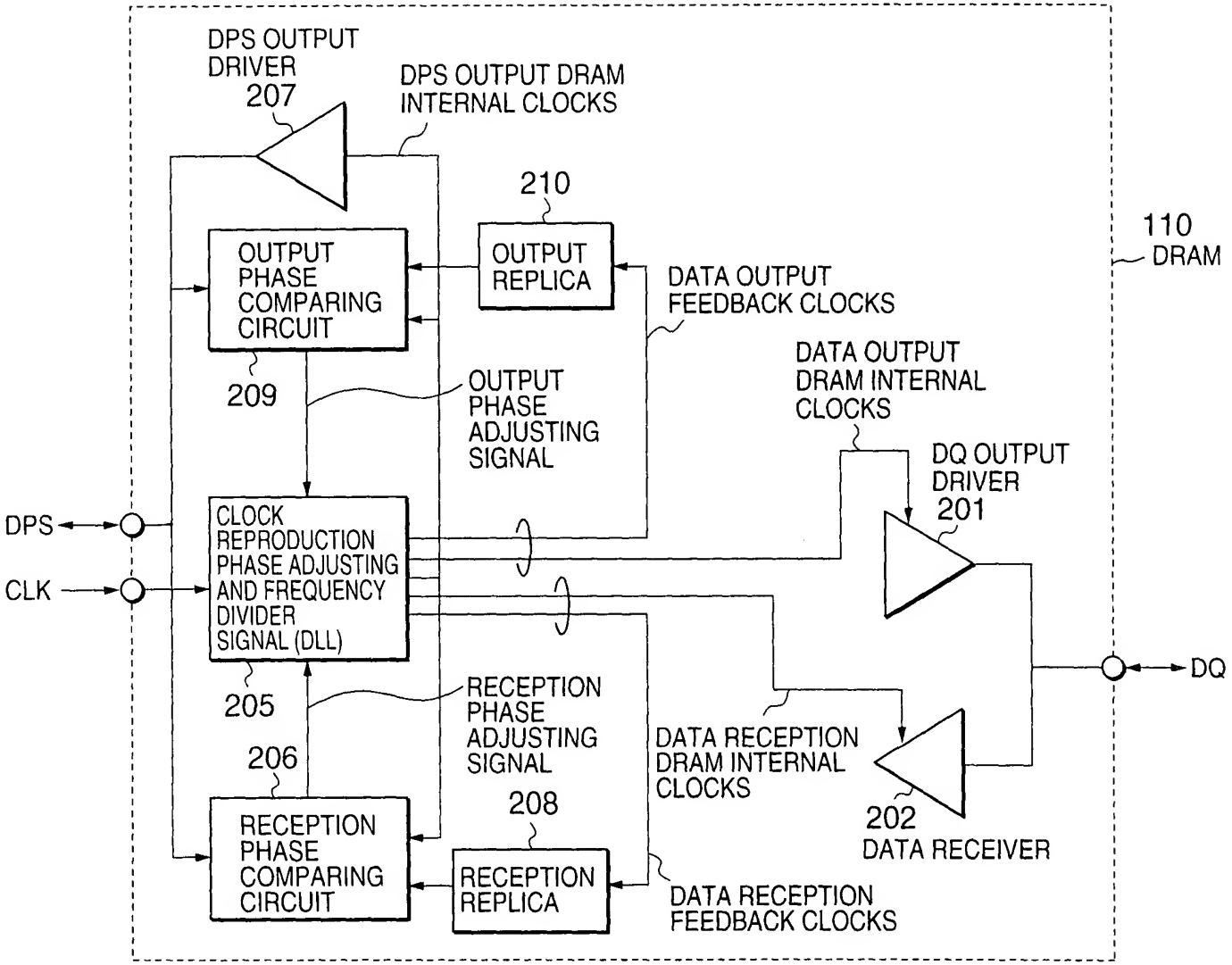

DPS OUTPUT DRIVER
207
DPS OUTPUT DRAM INTERNAL CLOCKS
210
110
DRAM
OUTPUT PHASE COMPARING CIRCUIT
OUTPUT REPLICA
DATA OUTPUT FEEDBACK CLOCKS
209
OUTPUT PHASE ADJUSTING SIGNAL
DATA OUTPUT DRAM INTERNAL CLOCKS
DQ OUTPUT DRIVER
201
DPS
CLK
CLOCK REPRODUCTION PHASE ADJUSTING AND FREQUENCY DIVIDER SIGNAL (DLL)
DQ
205
RECEPTION PHASE ADJUSTING SIGNAL
206
208
DATA RECEPTION DRAM INTERNAL CLOCKS
202
DATA RECEIVER
RECEPTION PHASE COMPARING CIRCUIT
RECEPTION REPLICA
DATA RECEPTION FEEDBACK CLOCKS

FIG.28

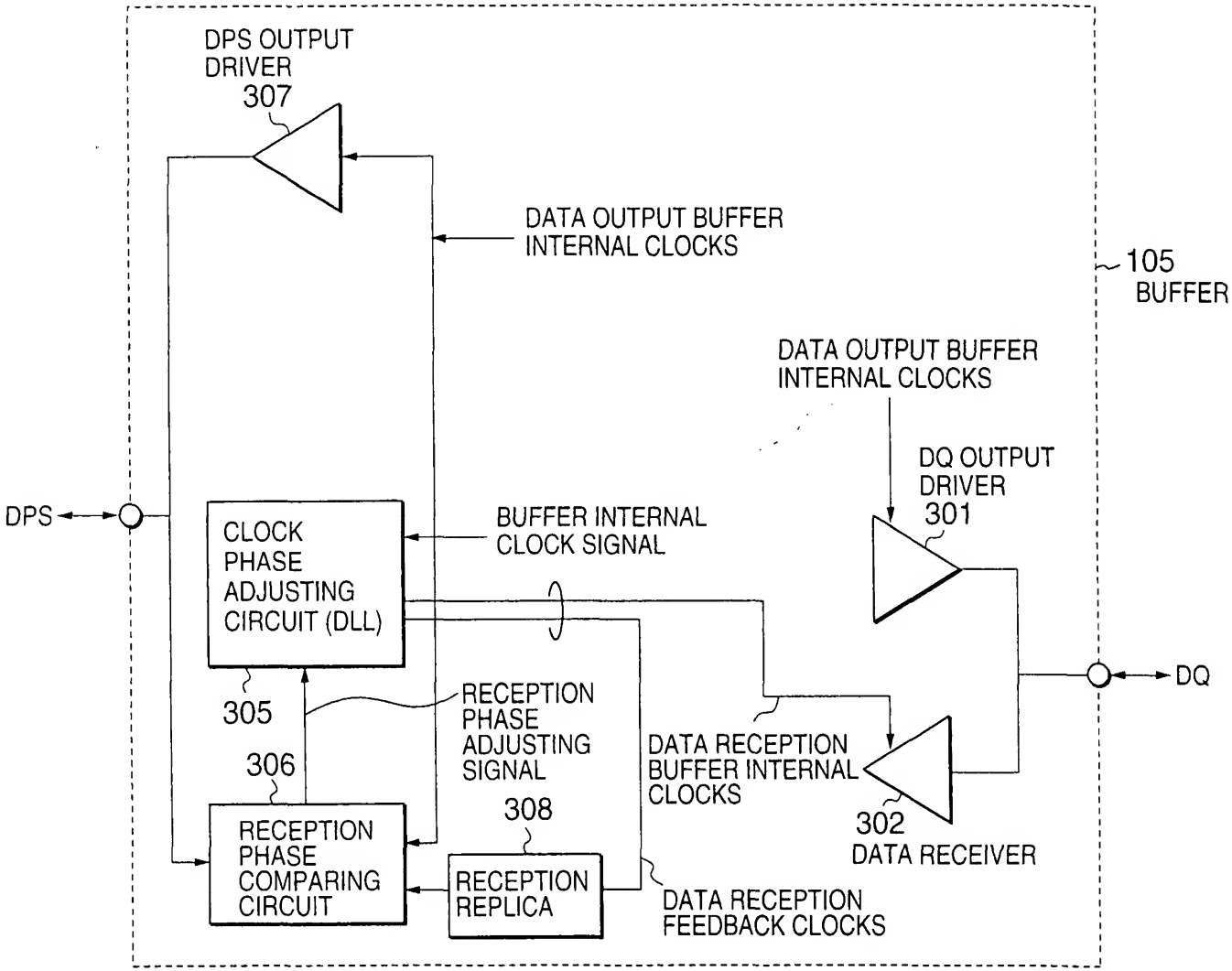

DPS OUTPUT
DRIVER
307
DATA OUTPUT BUFFER
INTERNAL CLOCKS
105
BUFFER
DATA OUTPUT BUFFER
INTERNAL CLOCKS
DQ OUTPUT
DRIVER
301
DPS
CLOCK
PHASE
ADJUSTING
CIRCUIT (DLL)
BUFFER INTERNAL
CLOCK SIGNAL
DQ
305
RECEPTION
PHASE
ADJUSTING
SIGNAL
306
308
DATA RECEPTION
BUFFER INTERNAL
CLOCKS
302
DATA RECEIVER
RECEPTION
PHASE
COMPARING
CIRCUIT
RECEPTION
REPLICA
DATA RECEPTION
FEEDBACK CLOCKS

FIG.29

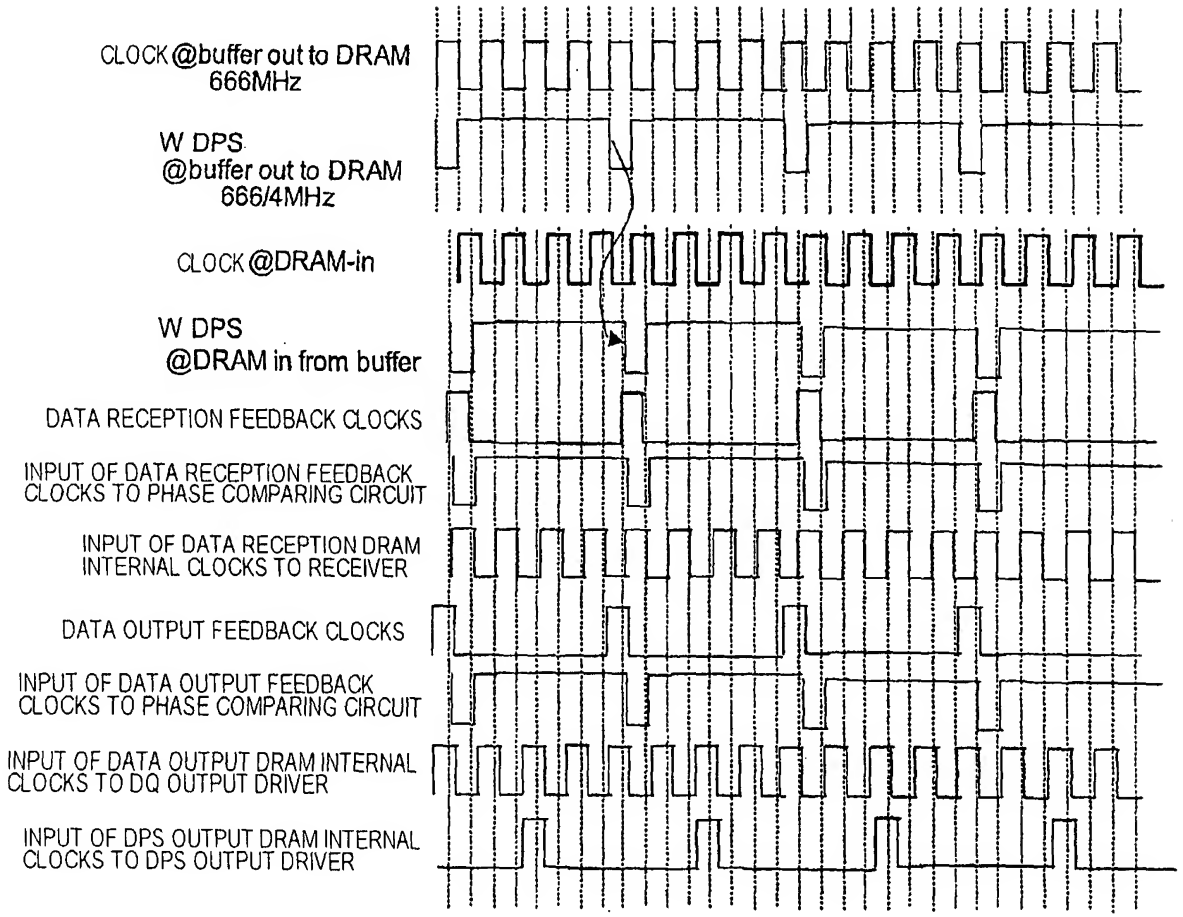

CLOCK @buffer out to DRAM 666MHz
W DPS @buffer out to DRAM 666/4MHz
CLOCK @DRAM-in
W DPS @DRAM in from buffer
DATA RECEPTION FEEDBACK CLOCKS
INPUT OF DATA RECEPTION FEEDBACK CLOCKS TO PHASE COMPARING CIRCUIT
INPUT OF DATA RECEPTION DRAM INTERNAL CLOCKS TO RECEIVER
DATA OUTPUT FEEDBACK CLOCKS
INPUT OF DATA OUTPUT FEEDBACK CLOCKS TO PHASE COMPARING CIRCUIT
INPUT OF DATA OUTPUT DRAM INTERNAL CLOCKS TO DQ OUTPUT DRIVER
INPUT OF DPS OUTPUT DRAM INTERNAL CLOCKS TO DPS OUTPUT DRIVER

FIG. 30

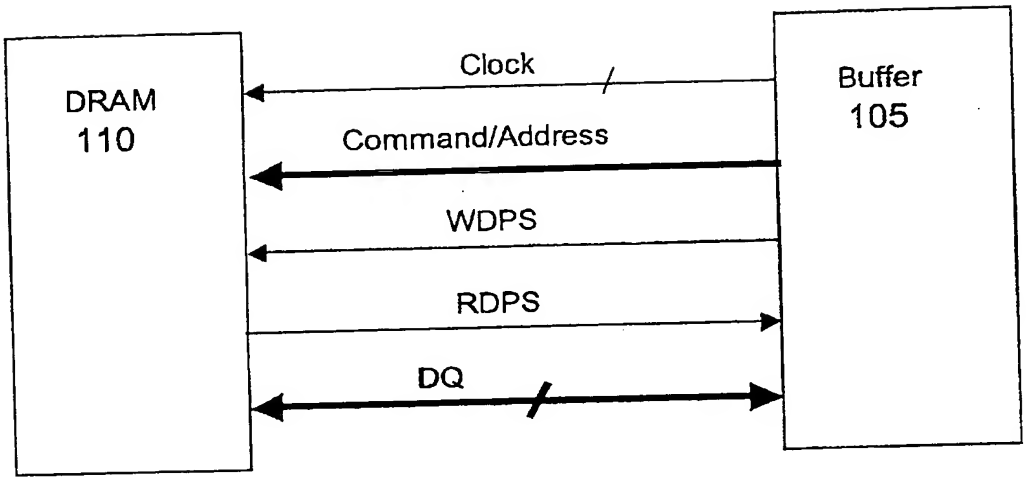


FIG. 31

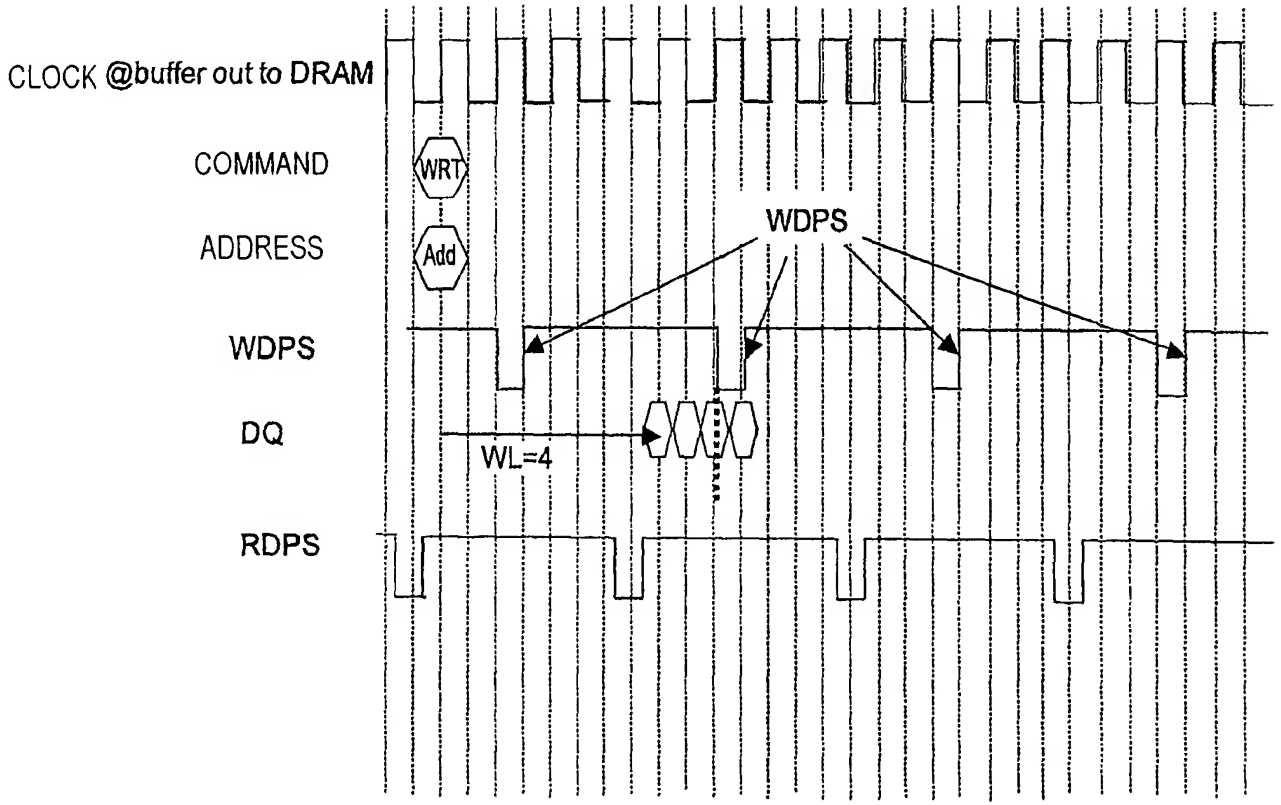

CLOCK @buffer out to DRAM
COMMAND
WRT
ADDRESS
Add
WDPS
WDPS
DQ
WL=4
RDPS

FIG. 32

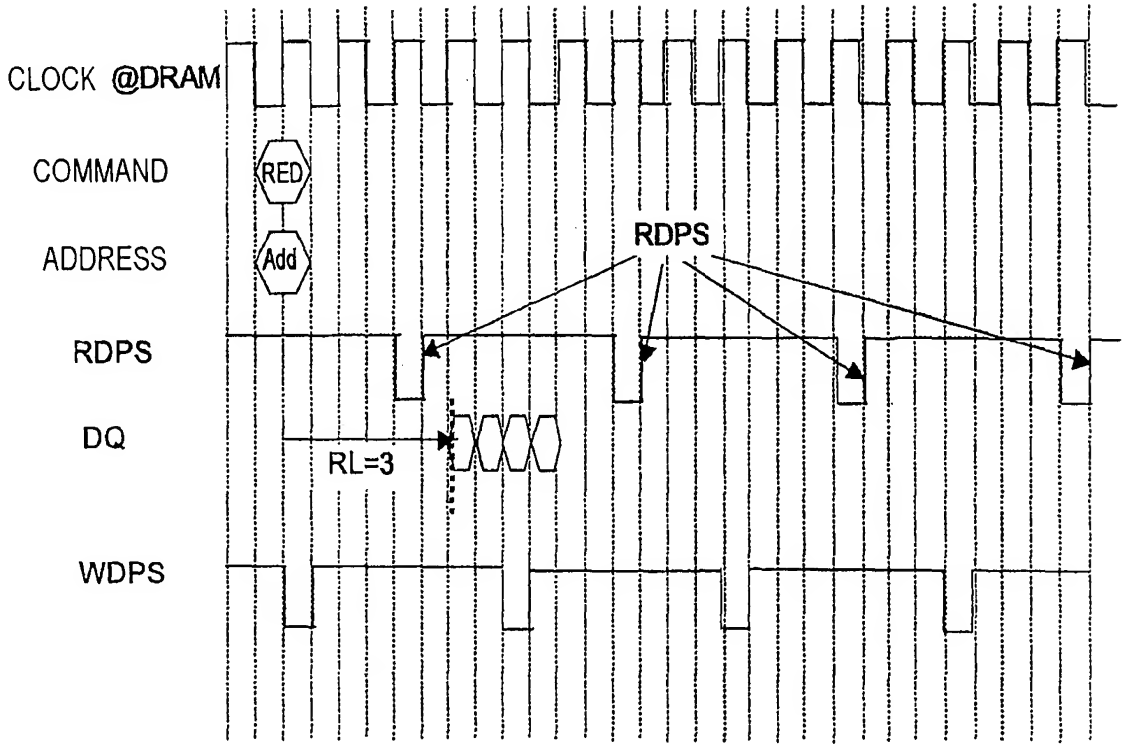


FIG. 33

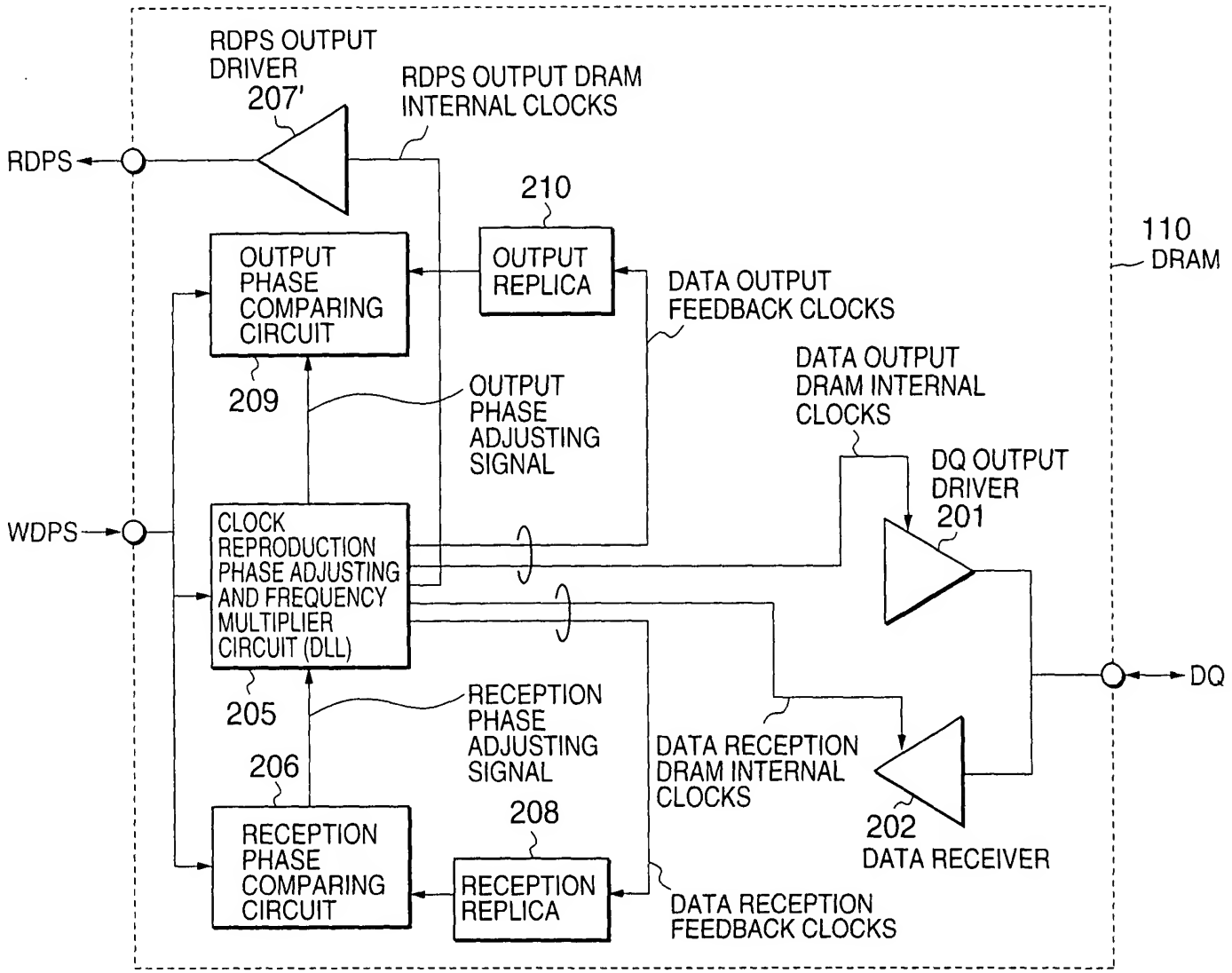

RDPS OUTPUT DRIVER
207'
RDPS OUTPUT DRAM INTERNAL CLOCKS
RDPS
210
OUTPUT REPLICA
110
DRAM
OUTPUT PHASE COMPARING CIRCUIT
DATA OUTPUT FEEDBACK CLOCKS
DATA OUTPUT DRAM INTERNAL CLOCKS
209
OUTPUT PHASE ADJUSTING SIGNAL
DQ OUTPUT DRIVER
201
WDPS
CLOCK REPRODUCTION PHASE ADJUSTING AND FREQUENCY MULTIPLIER CIRCUIT (DLL)
DQ
205
RECEPTION PHASE ADJUSTING SIGNAL
206
DATA RECEPTION DRAM INTERNAL CLOCKS
208
202
DATA RECEIVER
RECEPTION PHASE COMPARING CIRCUIT
RECEPTION REPLICA
DATA RECEPTION FEEDBACK CLOCKS

FIG.34

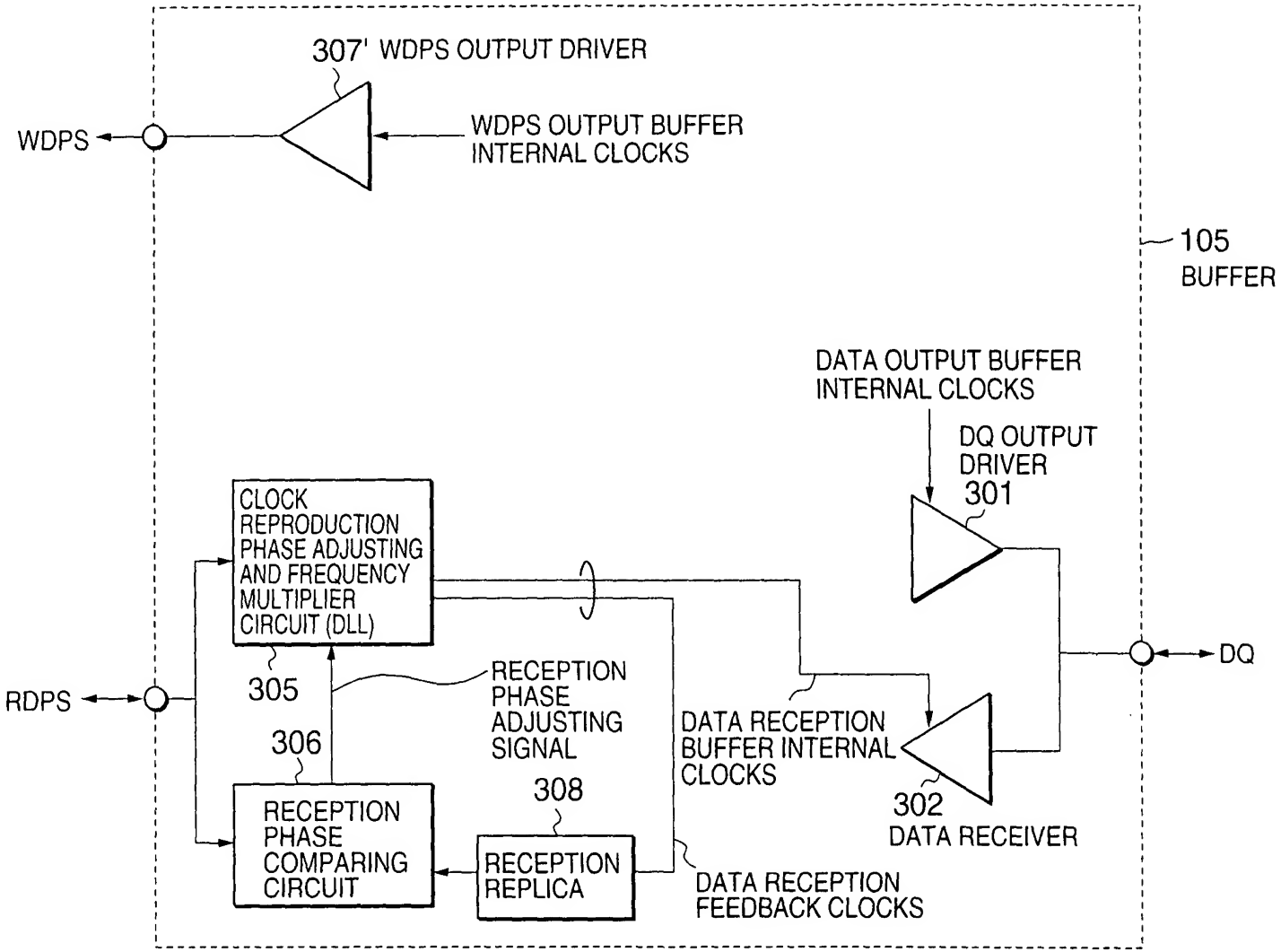

307' WDPS OUTPUT DRIVER
WDPS
WDPS OUTPUT BUFFER INTERNAL CLOCKS
105
BUFFER
DATA OUTPUT BUFFER INTERNAL CLOCKS
DQ OUTPUT DRIVER
301
CLOCK REPRODUCTION PHASE ADJUSTING AND FREQUENCY MULTIPLIER CIRCUIT (DLL)
305
RECEPTION PHASE ADJUSTING SIGNAL
RDPS
306
DATA RECEPTION BUFFER INTERNAL CLOCKS
DQ
308
RECEPTION PHASE COMPARING CIRCUIT
RECEPTION REPLICA
302
DATA RECEIVER
DATA RECEPTION FEEDBACK CLOCKS

FIG.35

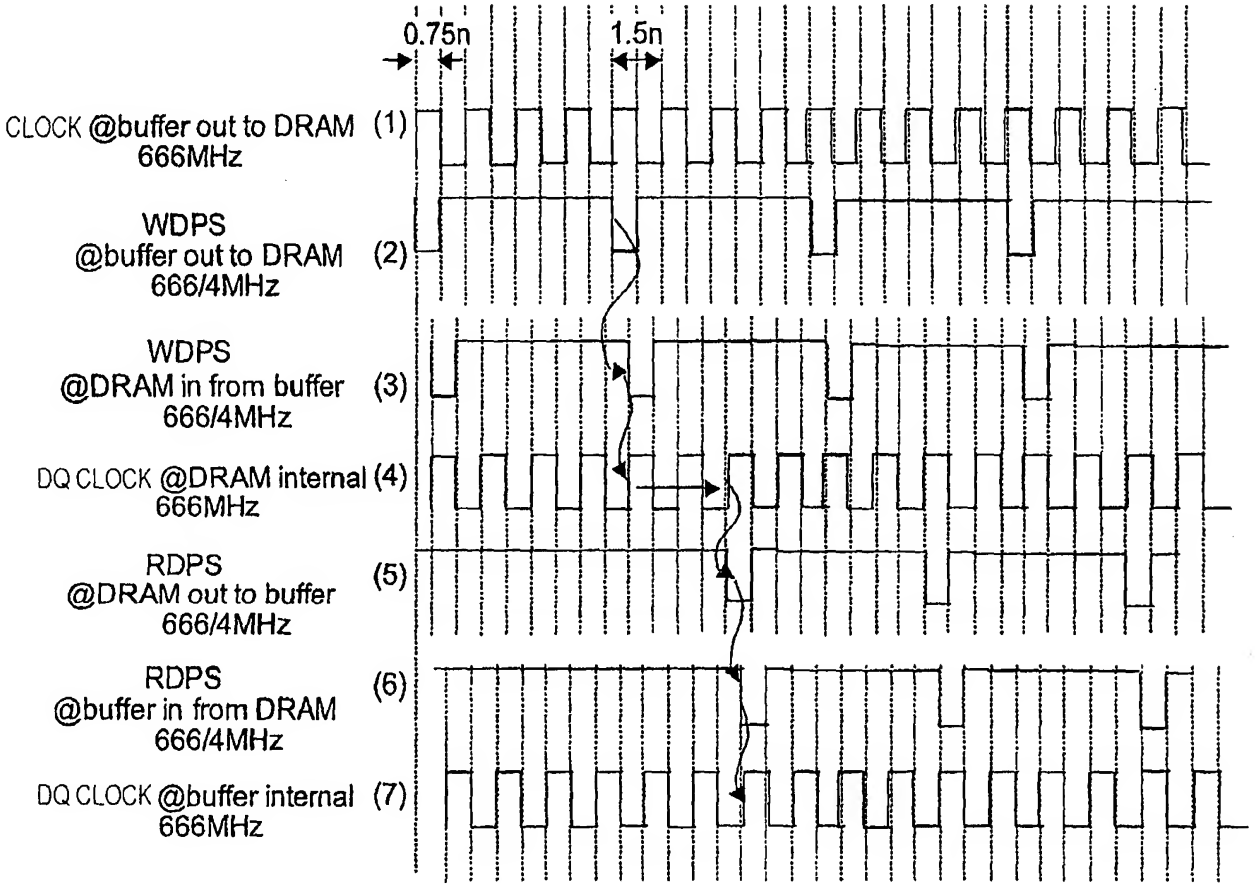

0.75n
1.5n
CLOCK @buffer out to DRAM 666MHz (1)
WDPS @buffer out to DRAM 666/4MHz (2)
WDPS @DRAM in from buffer 666/4MHz (3)
DQ CLOCK @DRAM internal 666MHz (4)
RDPS @DRAM out to buffer 666/4MHz (5)
RDPS @buffer in from DRAM 666/4MHz (6)
DQ CLOCK @buffer internal 666MHz (7)

FIG. 36

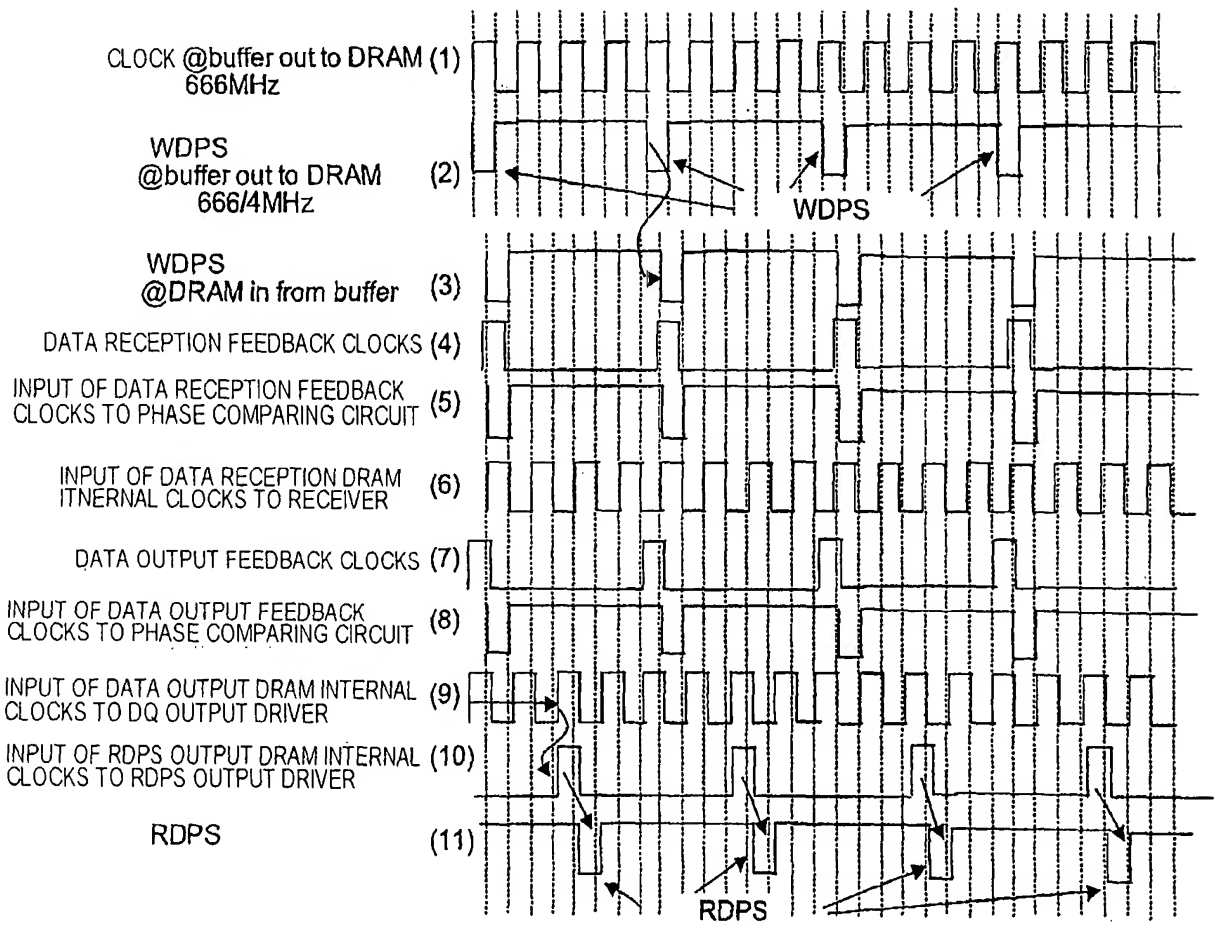

CLOCK @buffer out to DRAM (1)
666MHz
WDPS
@buffer out to DRAM (2)
666/4MHz
WDPS
WDPS
@DRAM in from buffer (3)
DATA RECEPTION FEEDBACK CLOCKS (4)
INPUT OF DATA RECEPTION FEEDBACK
CLOCKS TO PHASE COMPARING CIRCUIT (5)
INPUT OF DATA RECEPTION DRAM
ITNERNAL CLOCKS TO RECEIVER (6)
DATA OUTPUT FEEDBACK CLOCKS (7)
INPUT OF DATA OUTPUT FEEDBACK
CLOCKS TO PHASE COMPARING CIRCUIT (8)
INPUT OF DATA OUTPUT DRAM INTERNAL
CLOCKS TO DQ OUTPUT DRIVER (9)
INPUT OF RDPS OUTPUT DRAM INTERNAL
CLOCKS TO RDPS OUTPUT DRIVER (10)
RDPS (11)
RDPS

FIG. 37

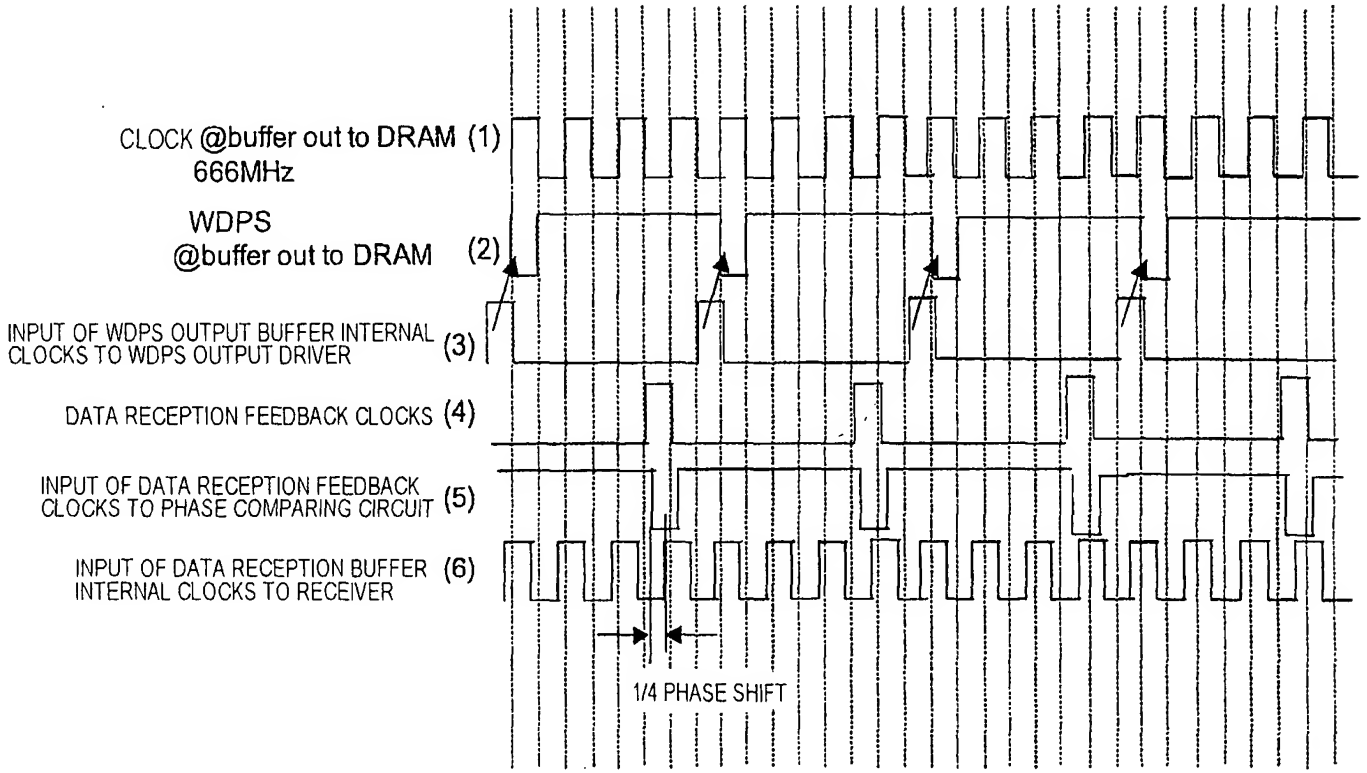

CLOCK @buffer out to DRAM (1)
666MHz
WDPS
@buffer out to DRAM (2)
INPUT OF WDPS OUTPUT BUFFER INTERNAL CLOCKS TO WDPS OUTPUT DRIVER (3)
DATA RECEPTION FEEDBACK CLOCKS (4)
INPUT OF DATA RECEPTION FEEDBACK CLOCKS TO PHASE COMPARING CIRCUIT (5)
INPUT OF DATA RECEPTION BUFFER INTERNAL CLOCKS TO RECEIVER (6)
1/4 PHASE SHIFT

FIG. 38

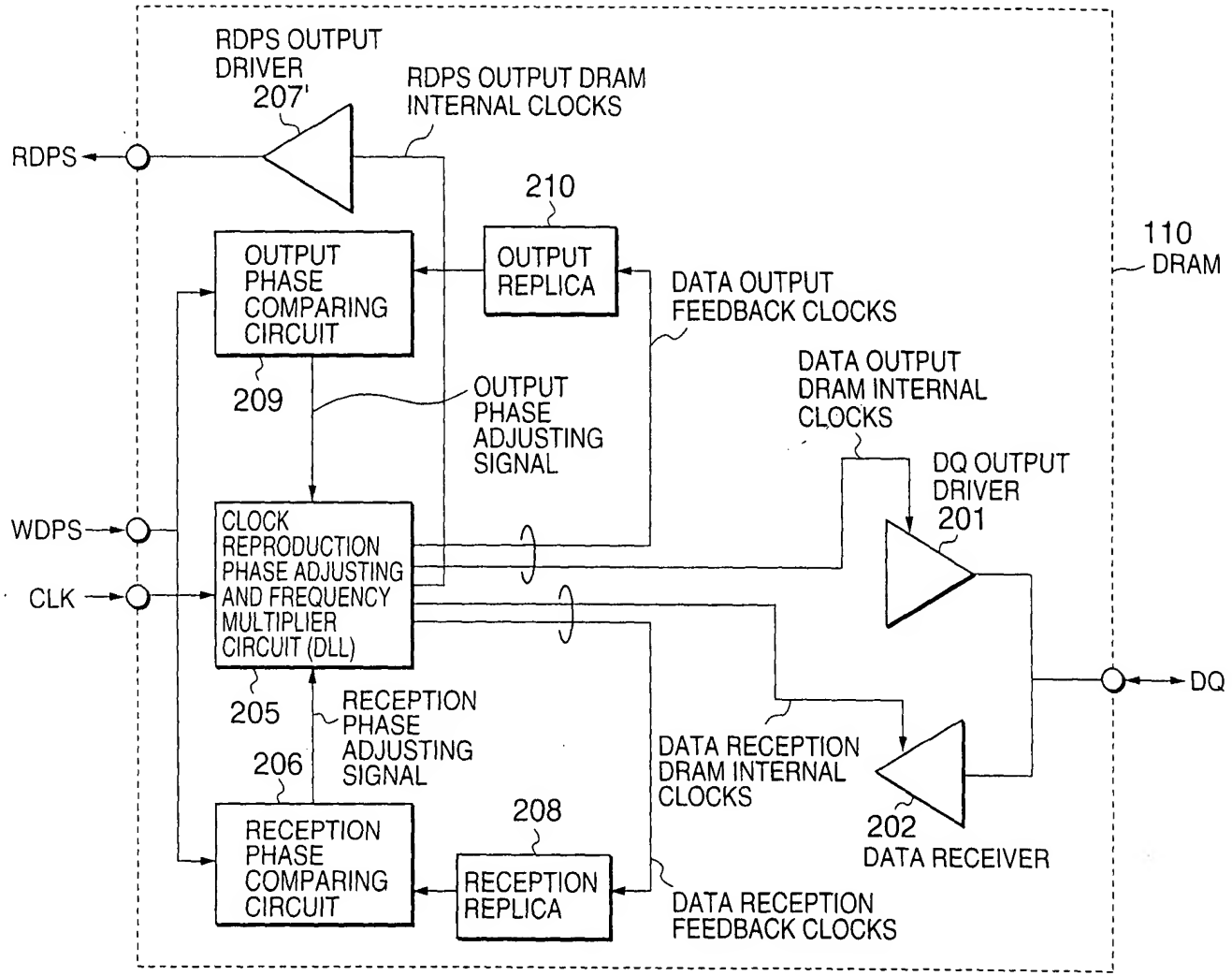

RDPS OUTPUT DRIVER
207'
RDPS OUTPUT DRAM INTERNAL CLOCKS
RDPS
210
OUTPUT REPLICA
110
DRAM
OUTPUT PHASE COMPARING CIRCUIT
DATA OUTPUT FEEDBACK CLOCKS
209
OUTPUT PHASE ADJUSTING SIGNAL
DATA OUTPUT DRAM INTERNAL CLOCKS
DQ OUTPUT DRIVER
201
WDPS
CLK
CLOCK REPRODUCTION PHASE ADJUSTING AND FREQUENCY MULTIPLIER CIRCUIT (DLL)
205
RECEPTION PHASE ADJUSTING SIGNAL
DQ
206
DATA RECEPTION DRAM INTERNAL CLOCKS
208
202
DATA RECEIVER
RECEPTION PHASE COMPARING CIRCUIT
RECEPTION REPLICA
DATA RECEPTION FEEDBACK CLOCKS

FIG.39

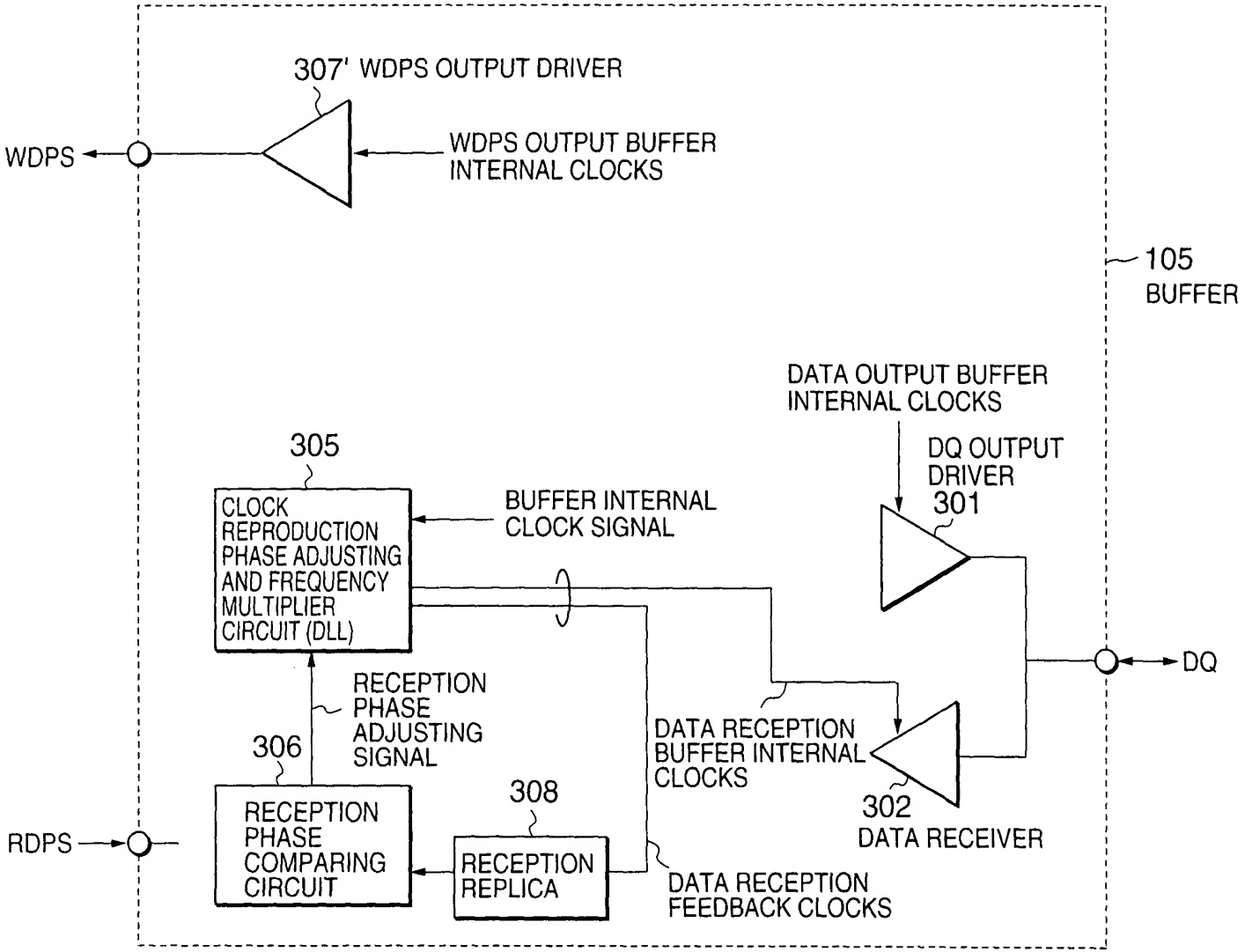

307' WDPS OUTPUT DRIVER
WDPS
WDPS OUTPUT BUFFER INTERNAL CLOCKS
105
BUFFER
DATA OUTPUT BUFFER INTERNAL CLOCKS
DQ OUTPUT DRIVER
301
305
CLOCK REPRODUCTION PHASE ADJUSTING AND FREQUENCY MULTIPLIER CIRCUIT (DLL)
BUFFER INTERNAL CLOCK SIGNAL
DQ
RECEPTION PHASE ADJUSTING SIGNAL
306
DATA RECEPTION BUFFER INTERNAL CLOCKS
308
302
DATA RECEIVER
RDPS
RECEPTION PHASE COMPARING CIRCUIT
RECEPTION REPLICA
DATA RECEPTION FEEDBACK CLOCKS

FIG.40

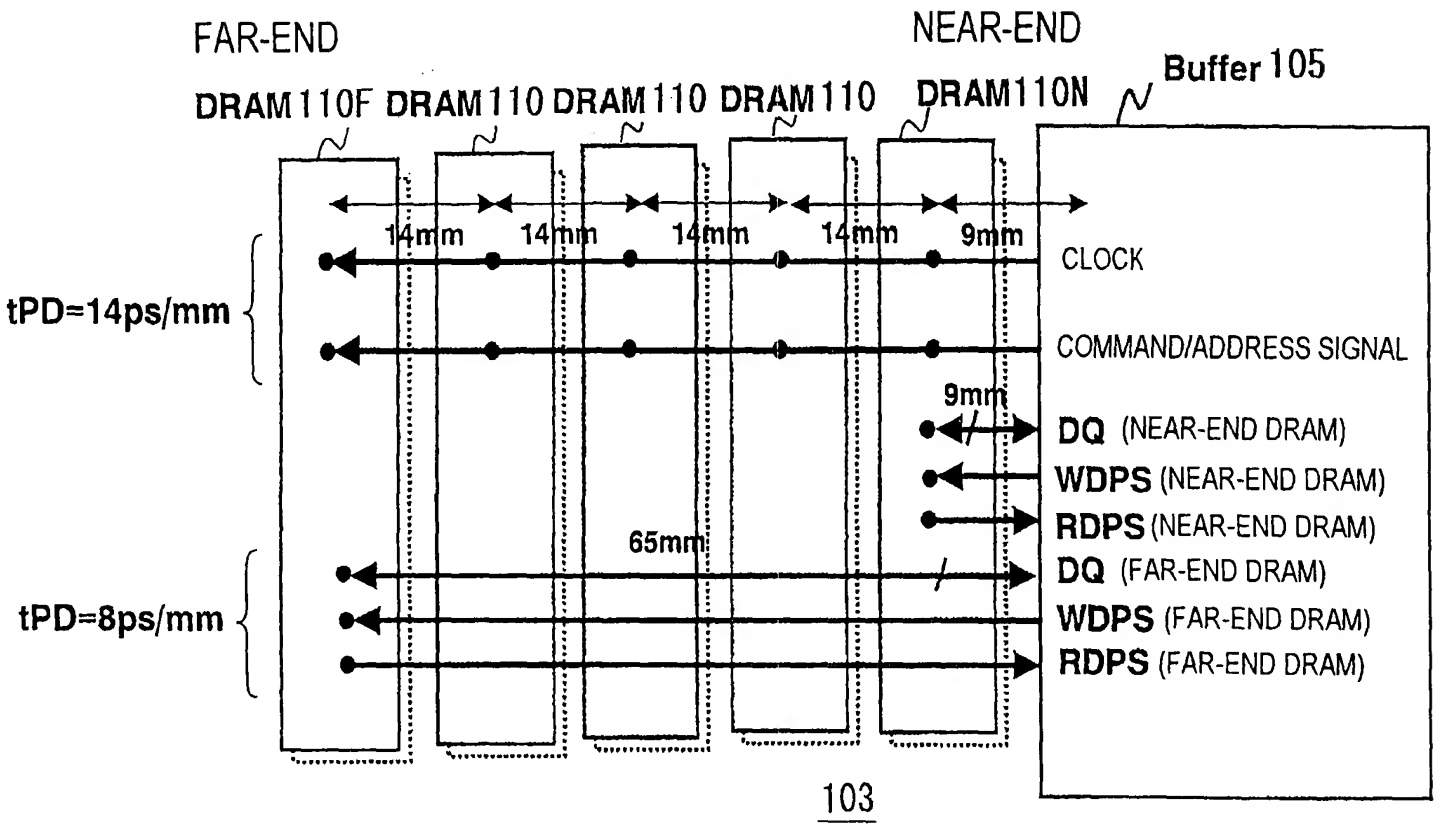

FAR-END
NEAR-END
DRAM 110F
DRAM 110
DRAM 110
DRAM 110
DRAM 110N
Buffer 105
14mm
14mm
14mm
14mm
9mm
tPD=14ps/mm
CLOCK
COMMAND/ADDRESS SIGNAL
9mm
DQ (NEAR-END DRAM)
WDPS (NEAR-END DRAM)
RDPS (NEAR-END DRAM)
65mm
tPD=8ps/mm
DQ (FAR-END DRAM)
WDPS (FAR-END DRAM)
RDPS (FAR-END DRAM)
103

FIG. 41

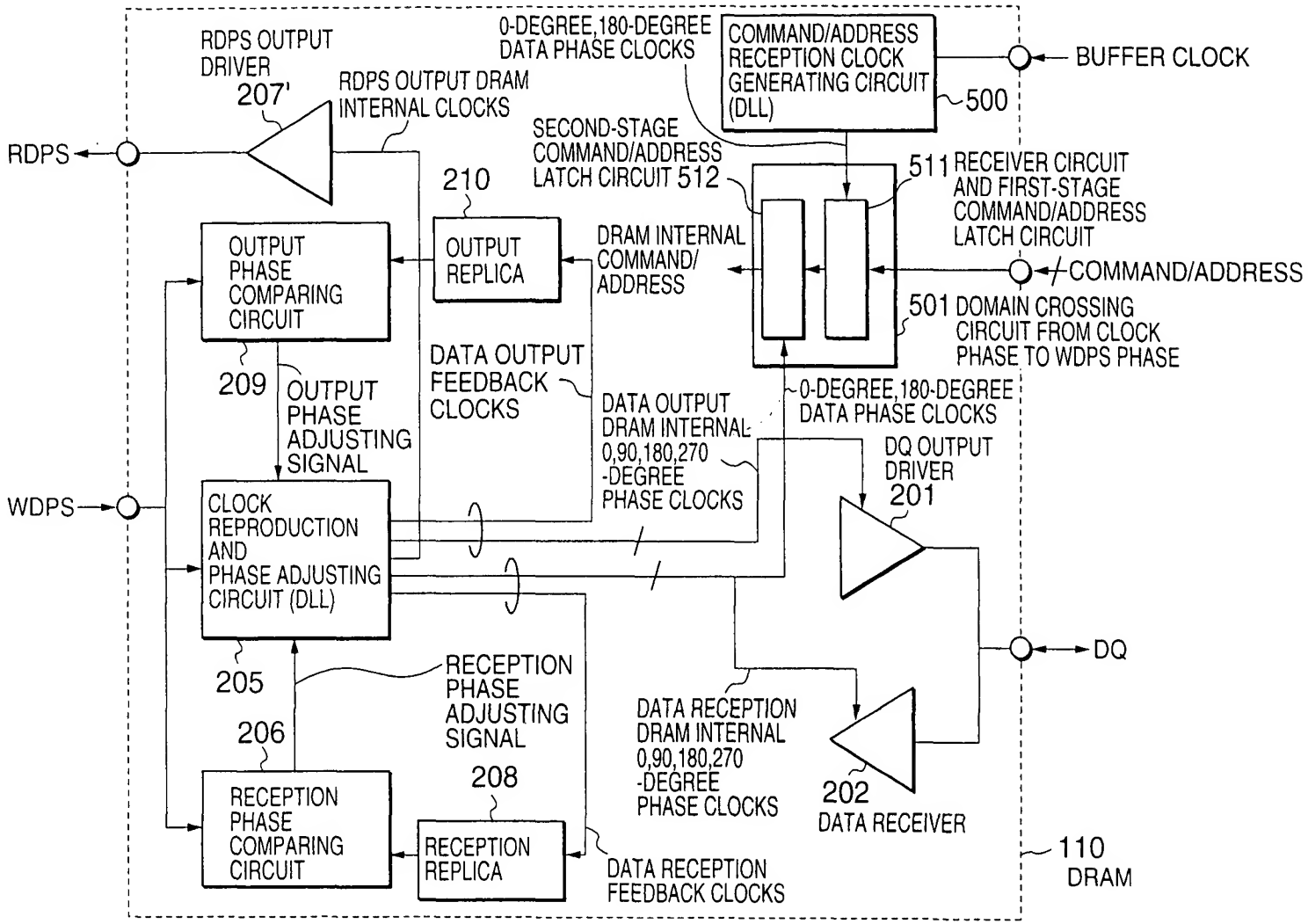

RDPS OUTPUT DRIVER
207'
RDPS OUTPUT DRAM INTERNAL CLOCKS
0-DEGREE,180-DEGREE DATA PHASE CLOCKS
COMMAND/ADDRESS RECEPTION CLOCK GENERATING CIRCUIT (DLL)
500
BUFFER CLOCK
RDPS
SECOND-STAGE COMMAND/ADDRESS LATCH CIRCUIT 512
511 RECEIVER CIRCUIT AND FIRST-STAGE COMMAND/ADDRESS LATCH CIRCUIT
210
OUTPUT REPLICA
DRAM INTERNAL COMMAND/ ADDRESS
COMMAND/ADDRESS
OUTPUT PHASE COMPARING CIRCUIT
501 DOMAIN CROSSING CIRCUIT FROM CLOCK PHASE TO WDPS PHASE
DATA OUTPUT FEEDBACK CLOCKS
209
OUTPUT PHASE ADJUSTING SIGNAL
0-DEGREE,180-DEGREE DATA PHASE CLOCKS
DATA OUTPUT DRAM INTERNAL 0,90,180,270 -DEGREE PHASE CLOCKS
DQ OUTPUT DRIVER
201
WDPS
CLOCK REPRODUCTION AND PHASE ADJUSTING CIRCUIT (DLL)
DQ
205
RECEPTION PHASE ADJUSTING SIGNAL
206
DATA RECEPTION DRAM INTERNAL 0,90,180,270 -DEGREE PHASE CLOCKS
202
DATA RECEIVER
208
RECEPTION PHASE COMPARING CIRCUIT
RECEPTION REPLICA
DATA RECEPTION FEEDBACK CLOCKS
110
DRAM

FIG.42

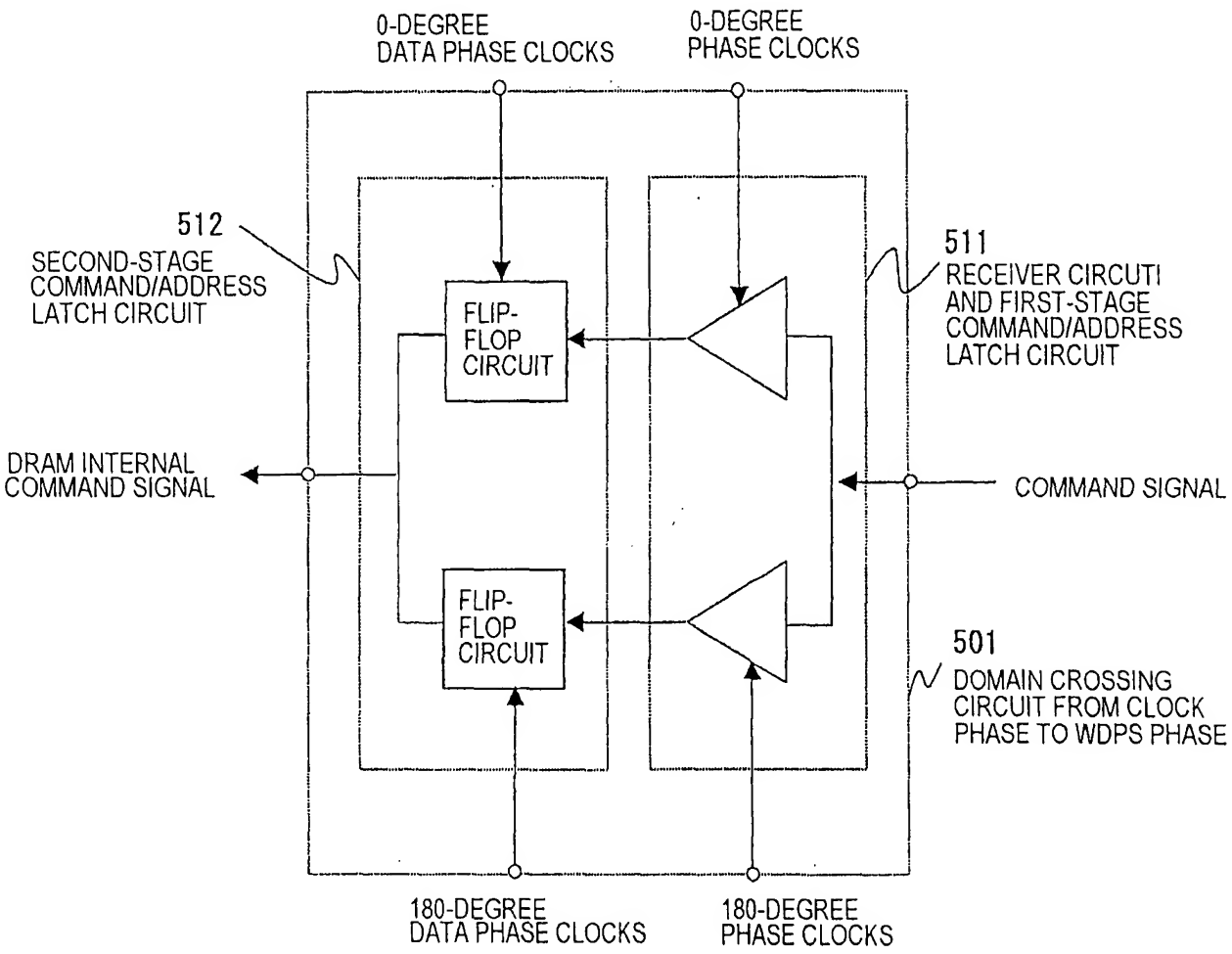

0-DEGREE
DATA PHASE CLOCKS
0-DEGREE
PHASE CLOCKS
512
SECOND-STAGE
COMMAND/ADDRESS
LATCH CIRCUIT
511
RECEIVER CIRCUIT
AND FIRST-STAGE
COMMAND/ADDRESS
LATCH CIRCUIT
FLIP-
FLOP
CIRCUIT
DRAM INTERNAL
COMMAND SIGNAL
COMMAND SIGNAL
FLIP-
FLOP
CIRCUIT
501
DOMAIN CROSSING
CIRCUIT FROM CLOCK
PHASE TO WDPS PHASE
180-DEGREE
DATA PHASE CLOCKS
180-DEGREE
PHASE CLOCKS

FIG. 43

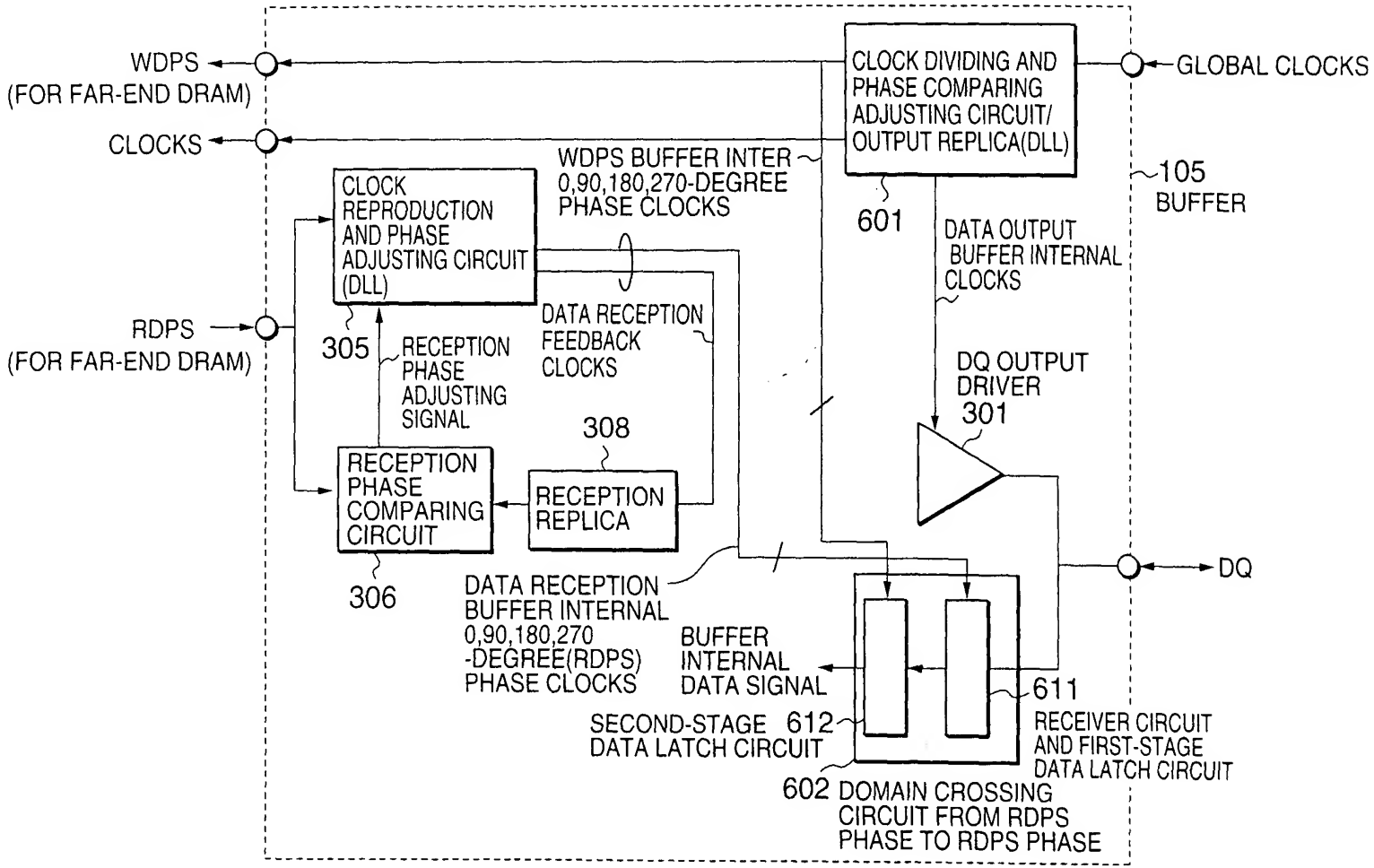

WDPS
(FOR FAR-END DRAM)
CLOCKS
RDPS
(FOR FAR-END DRAM)
CLOCK DIVIDING AND PHASE COMPARING ADJUSTING CIRCUIT/ OUTPUT REPLICA(DLL)
GLOBAL CLOCKS
WDPS BUFFER INTER 0,90,180,270-DEGREE PHASE CLOCKS
601
105 BUFFER
DATA OUTPUT BUFFER INTERNAL CLOCKS
CLOCK REPRODUCTION AND PHASE ADJUSTING CIRCUIT (DLL)
305
RECEPTION PHASE ADJUSTING SIGNAL
DATA RECEPTION FEEDBACK CLOCKS
DQ OUTPUT DRIVER
301
308
RECEPTION PHASE COMPARING CIRCUIT
RECEPTION REPLICA
306
DQ
DATA RECEPTION BUFFER INTERNAL 0,90,180,270 -DEGREE(RDPS) PHASE CLOCKS
BUFFER INTERNAL DATA SIGNAL
611
SECOND-STAGE DATA LATCH CIRCUIT
612
RECEIVER CIRCUIT AND FIRST-STAGE DATA LATCH CIRCUIT
602 DOMAIN CROSSING CIRCUIT FROM RDPS PHASE TO RDPS PHASE

FIG.44

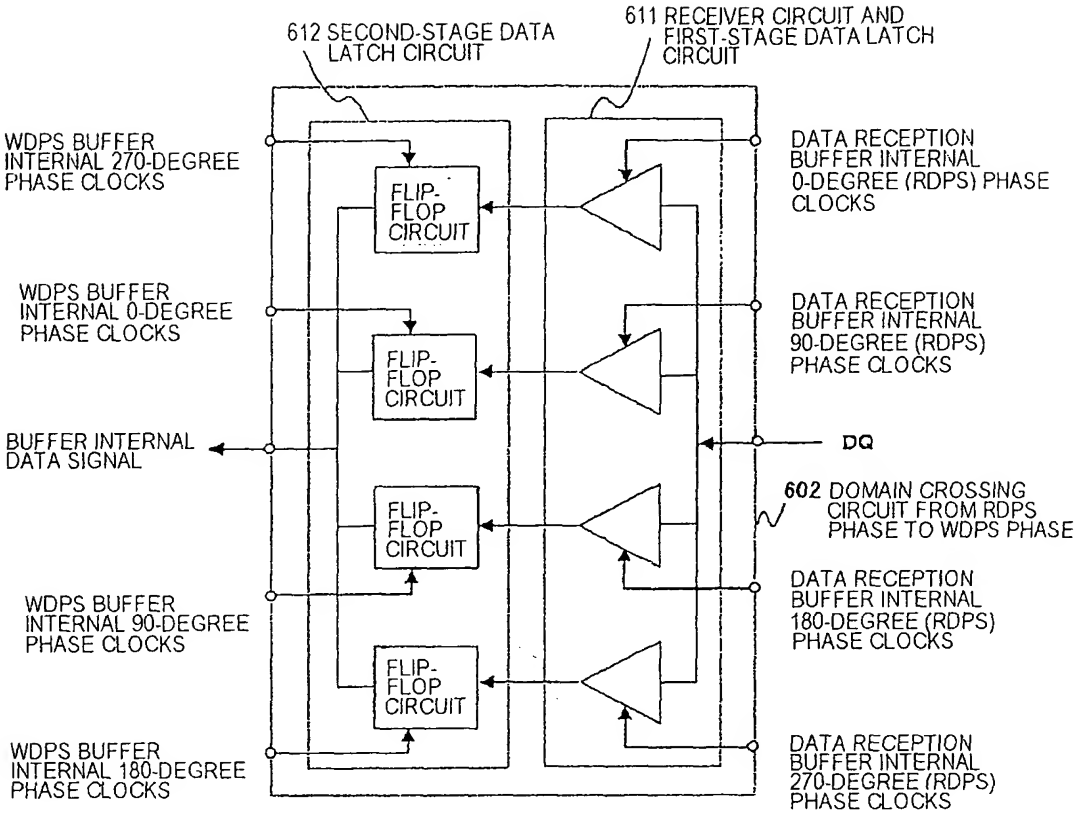

612 SECOND-STAGE DATA LATCH CIRCUIT
611 RECEIVER CIRCUIT AND FIRST-STAGE DATA LATCH CIRCUIT
WDPS BUFFER INTERNAL 270-DEGREE PHASE CLOCKS
WDPS BUFFER INTERNAL 0-DEGREE PHASE CLOCKS
BUFFER INTERNAL DATA SIGNAL
WDPS BUFFER INTERNAL 90-DEGREE PHASE CLOCKS
WDPS BUFFER INTERNAL 180-DEGREE PHASE CLOCKS
FLIP-FLOP CIRCUIT
FLIP-FLOP CIRCUIT
FLIP-FLOP CIRCUIT
FLIP-FLOP CIRCUIT
DATA RECEPTION BUFFER INTERNAL 0-DEGREE (RDPS) PHASE CLOCKS
DATA RECEPTION BUFFER INTERNAL 90-DEGREE (RDPS) PHASE CLOCKS
DQ
602 DOMAIN CROSSING CIRCUIT FROM RDPS PHASE TO WDPS PHASE
DATA RECEPTION BUFFER INTERNAL 180-DEGREE (RDPS) PHASE CLOCKS
DATA RECEPTION BUFFER INTERNAL 270-DEGREE (RDPS) PHASE CLOCKS

FIG. 45

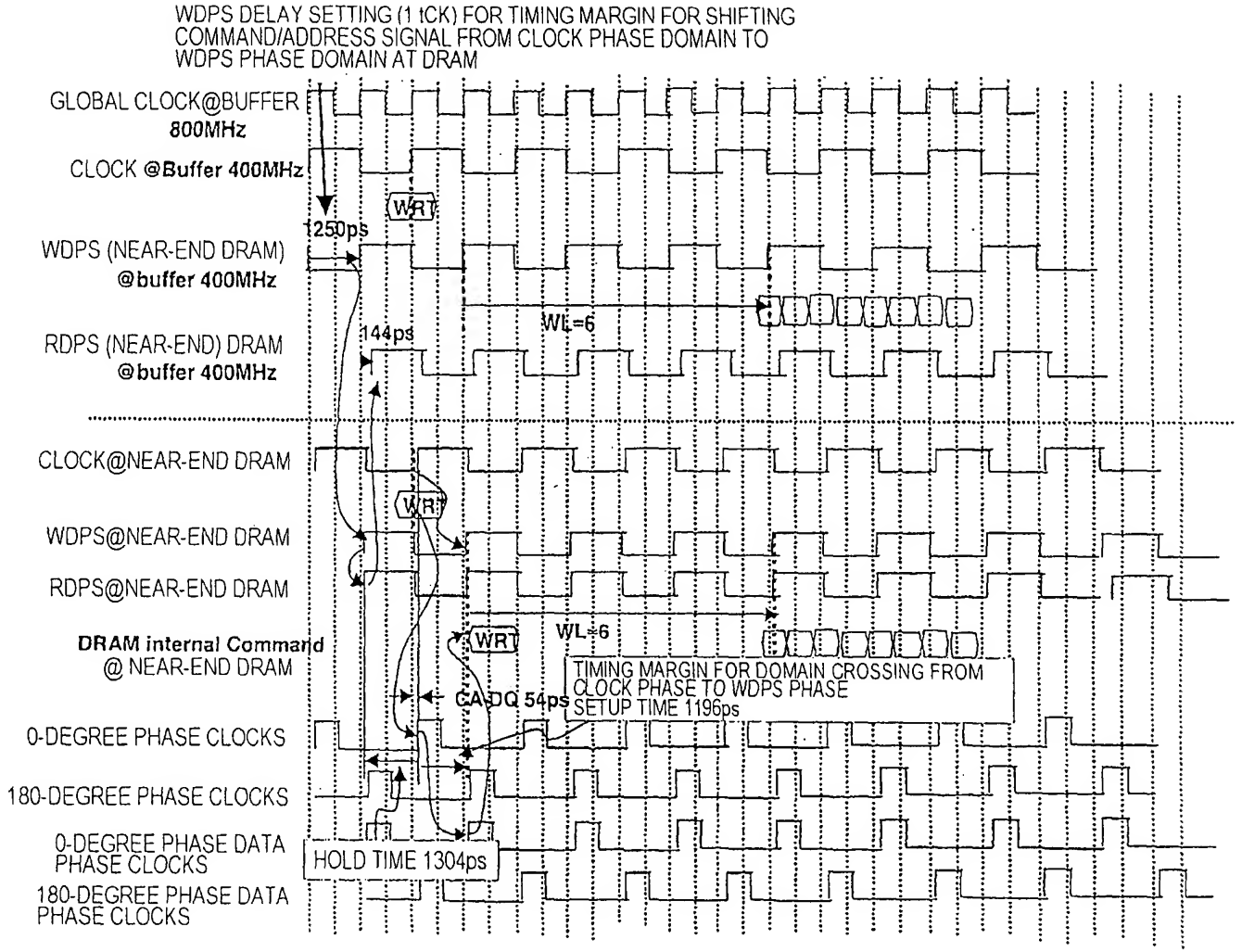

WDPS DELAY SETTING (1 tCK) FOR TIMING MARGIN FOR SHIFTING COMMAND/ADDRESS SIGNAL FROM CLOCK PHASE DOMAIN TO WDPS PHASE DOMAIN AT DRAM
GLOBAL CLOCK@BUFFER 800MHz
CLOCK @Buffer 400MHz
WRT
1250ps
WDPS (NEAR-END DRAM) @buffer 400MHz
WL=6
144ps
RDPS (NEAR-END) DRAM @buffer 400MHz
CLOCK@NEAR-END DRAM
WRT
WDPS@NEAR-END DRAM
RDPS@NEAR-END DRAM
DRAM internal Command @ NEAR-END DRAM
WRT
WL=6
TIMING MARGIN FOR DOMAIN CROSSING FROM CLOCK PHASE TO WDPS PHASE SETUP TIME 1196ps
CA-DQ 54ps
0-DEGREE PHASE CLOCKS
180-DEGREE PHASE CLOCKS
0-DEGREE PHASE DATA PHASE CLOCKS
HOLD TIME 1304ps
180-DEGREE PHASE DATA PHASE CLOCKS

FIG. 46

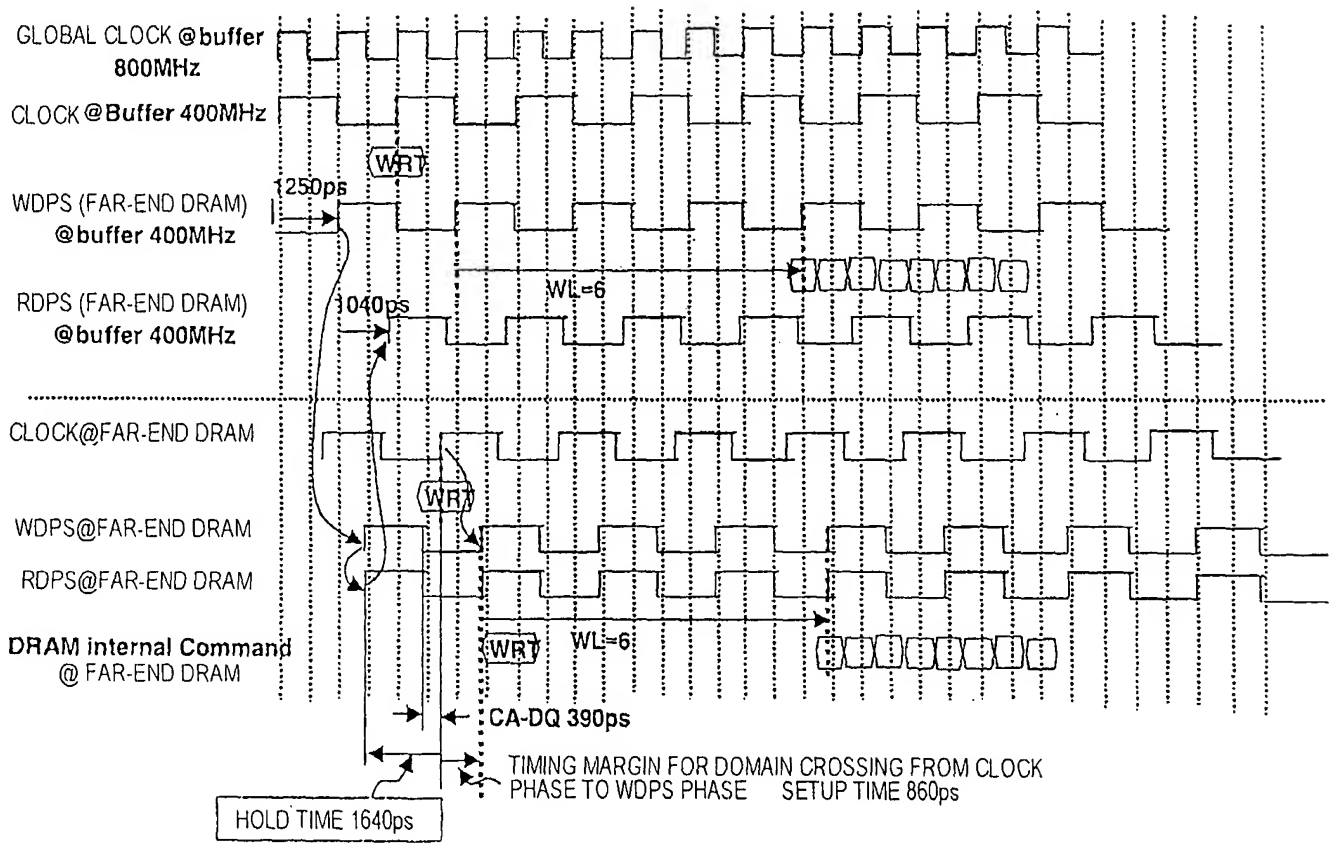

GLOBAL CLOCK @buffer 800MHz
CLOCK @Buffer 400MHz
WRT
1250ps
WDPS (FAR-END DRAM) @buffer 400MHz
WL=6
1040ps
RDPS (FAR-END DRAM) @buffer 400MHz
CLOCK@FAR-END DRAM
WRT
WDPS@FAR-END DRAM
RDPS@FAR-END DRAM
DRAM internal Command @ FAR-END DRAM
WRT
WL=6
CA-DQ 390ps
TIMING MARGIN FOR DOMAIN CROSSING FROM CLOCK PHASE TO WDPS PHASE
SETUP TIME 860ps
HOLD TIME 1640ps

FIG. 47

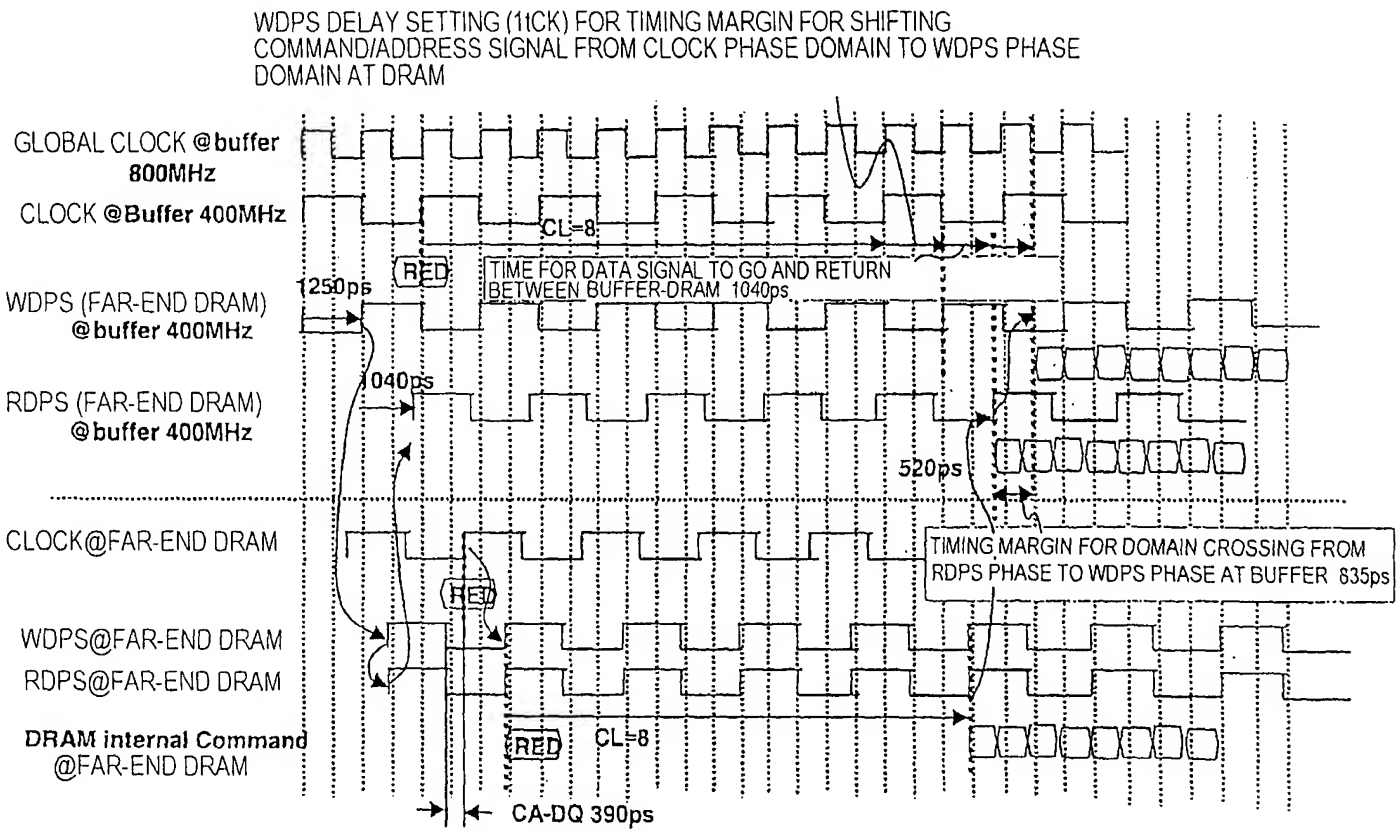

WDPS DELAY SETTING (11CK) FOR TIMING MARGIN FOR SHIFTING COMMAND/ADDRESS SIGNAL FROM CLOCK PHASE DOMAIN TO WDPS PHASE DOMAIN AT DRAM
GLOBAL CLOCK @buffer 800MHz
CLOCK @Buffer 400MHz
CL=8
RED
TIME FOR DATA SIGNAL TO GO AND RETURN BETWEEN BUFFER-DRAM 1040ps
WDPS (FAR-END DRAM) @buffer 400MHz
1250ps
1040ps
RDPS (FAR-END DRAM) @buffer 400MHz
520ps
CLOCK@FAR-END DRAM
TIMING MARGIN FOR DOMAIN CROSSING FROM RDPS PHASE TO WDPS PHASE AT BUFFER 835ps
RED
WDPS@FAR-END DRAM
RDPS@FAR-END DRAM
DRAM internal Command @FAR-END DRAM
RED
CL=8
CA-DQ 390ps

FIG. 48

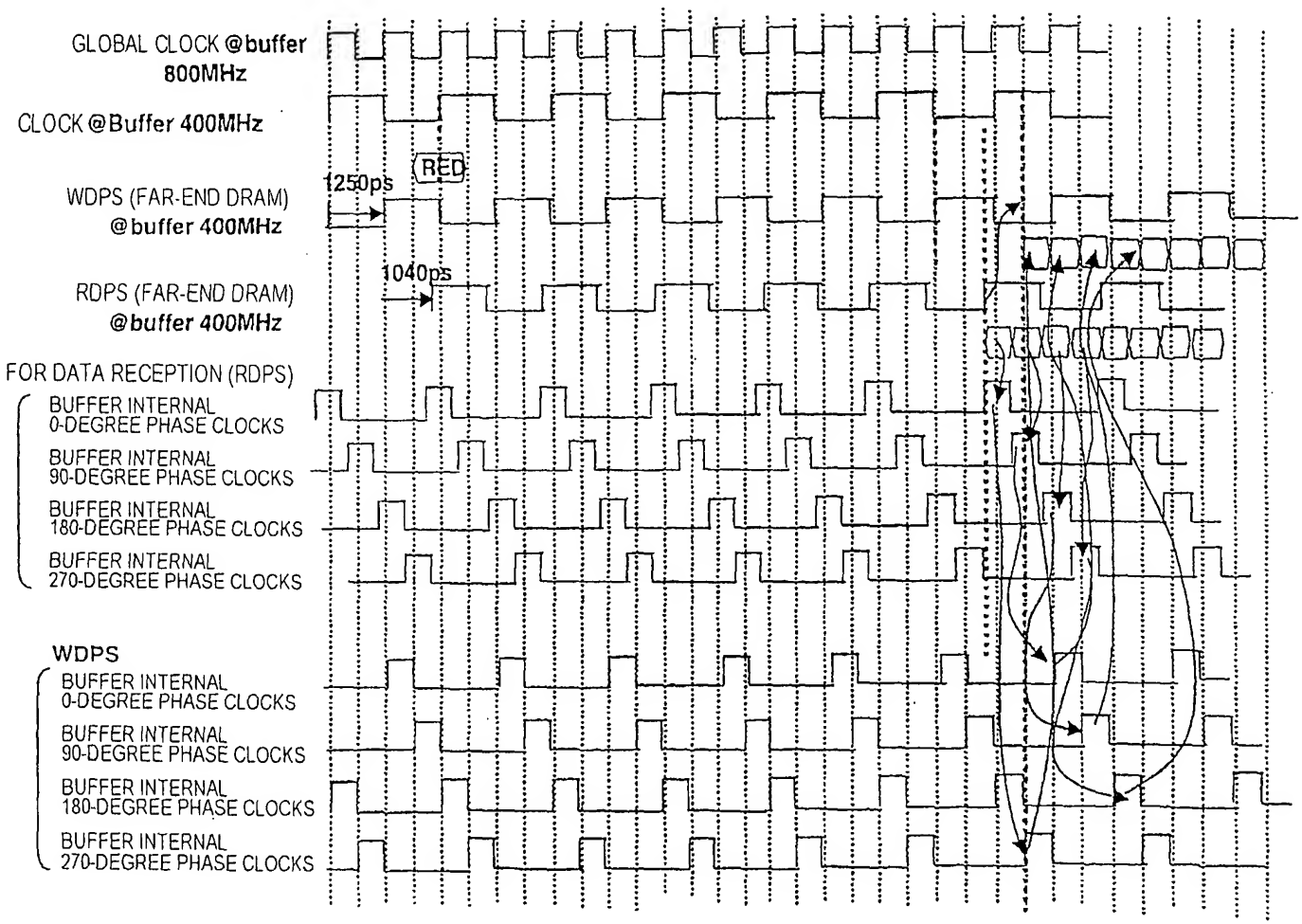

GLOBAL CLOCK @buffer 800MHz
CLOCK @Buffer 400MHz
WDPS (FAR-END DRAM) @buffer 400MHz
1250ps
RED
RDPS (FAR-END DRAM) @buffer 400MHz
1040ps
FOR DATA RECEPTION (RDPS)
BUFFER INTERNAL 0-DEGREE PHASE CLOCKS
BUFFER INTERNAL 90-DEGREE PHASE CLOCKS
BUFFER INTERNAL 180-DEGREE PHASE CLOCKS
BUFFER INTERNAL 270-DEGREE PHASE CLOCKS
WDPS
BUFFER INTERNAL 0-DEGREE PHASE CLOCKS
BUFFER INTERNAL 90-DEGREE PHASE CLOCKS
BUFFER INTERNAL 180-DEGREE PHASE CLOCKS
BUFFER INTERNAL 270-DEGREE PHASE CLOCKS

FIG. 49

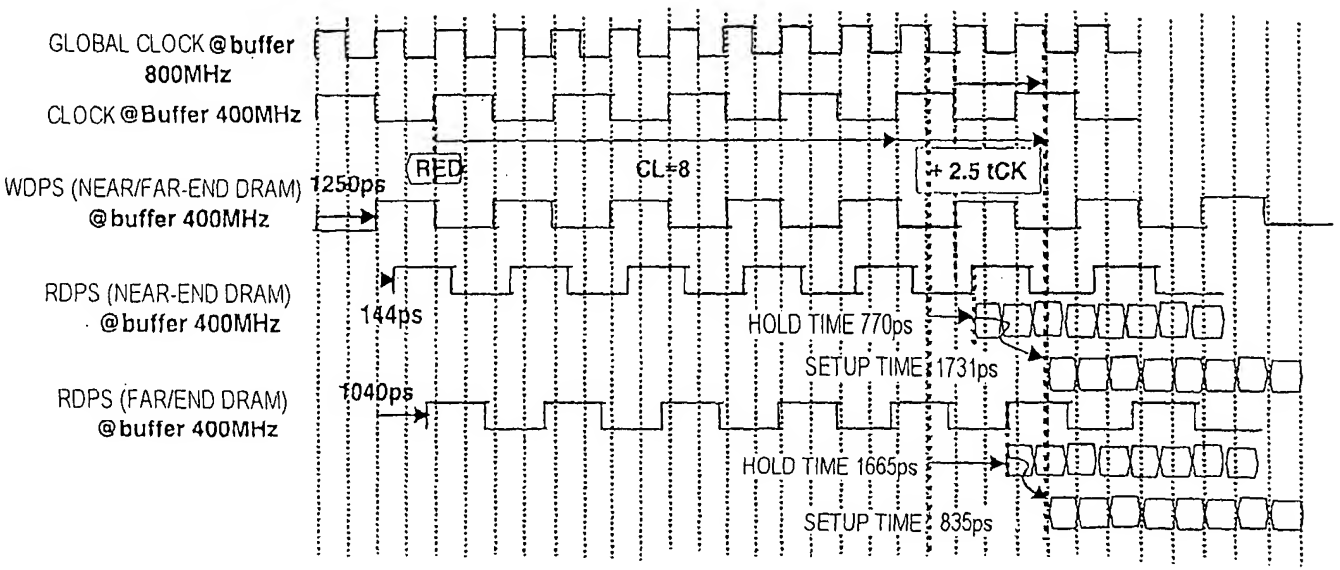

GLOBAL CLOCK @buffer 800MHz
CLOCK @Buffer 400MHz
WDPS (NEAR/FAR-END DRAM) @buffer 400MHz
RDPS (NEAR-END DRAM) @buffer 400MHz
RDPS (FAR/END DRAM) @buffer 400MHz
1250ps
RED
CL=8
+ 2.5 tCK
144ps
HOLD TIME 770ps
SETUP TIME 1731ps
1040ps
HOLD TIME 1665ps
SETUP TIME 835ps

FIG. 50

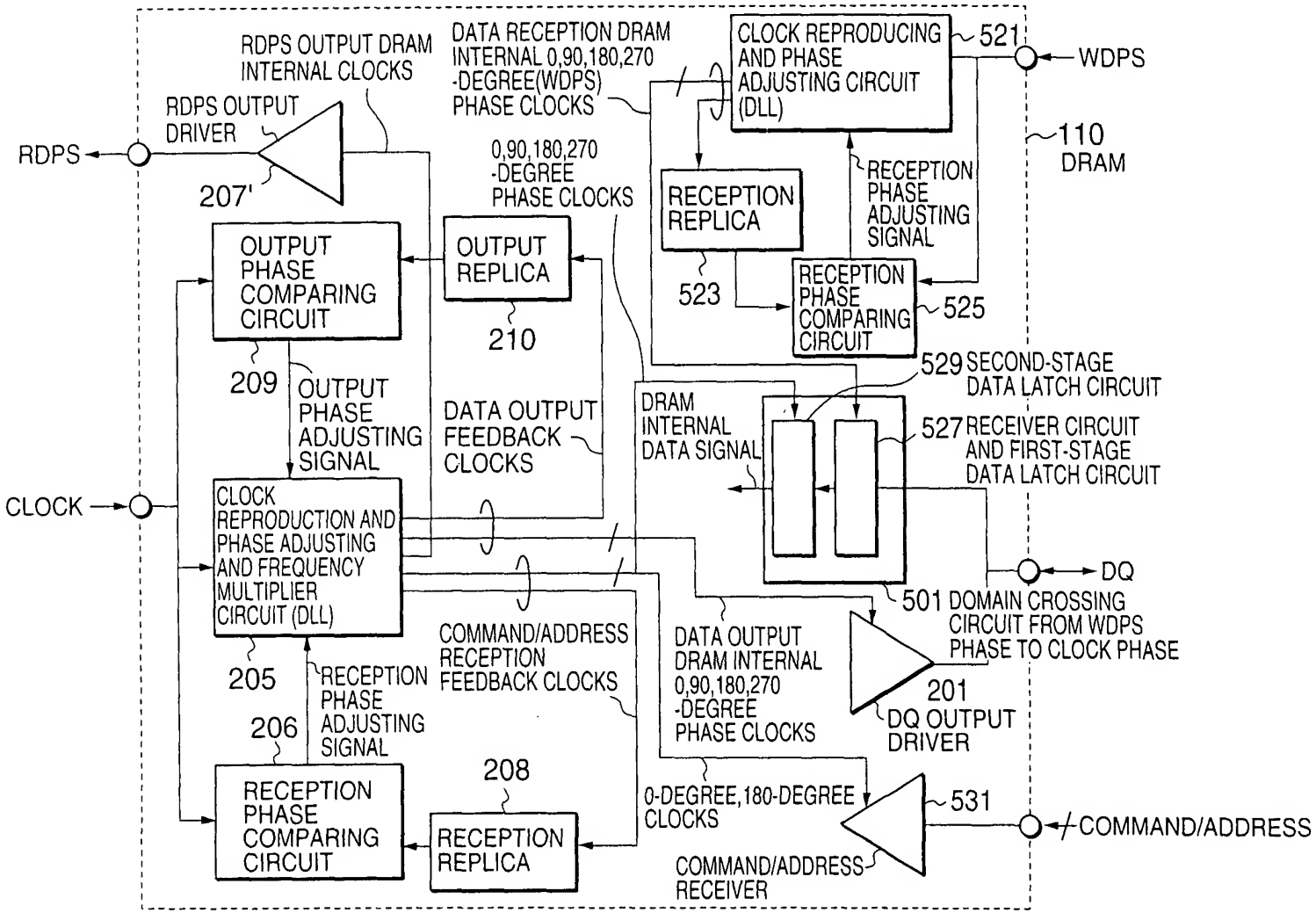

RDPS OUTPUT DRAM INTERNAL CLOCKS
DATA RECEPTION DRAM INTERNAL 0,90,180,270 -DEGREE(WDPS) PHASE CLOCKS
CLOCK REPRODUCING AND PHASE ADJUSTING CIRCUIT (DLL)
521
WDPS
RDPS OUTPUT DRIVER
RDPS
207'
0,90,180,270 -DEGREE PHASE CLOCKS
110 DRAM
RECEPTION REPLICA
RECEPTION PHASE ADJUSTING SIGNAL
OUTPUT PHASE COMPARING CIRCUIT
OUTPUT REPLICA
523
RECEPTION PHASE COMPARING CIRCUIT
525
210
209
OUTPUT PHASE ADJUSTING SIGNAL
529 SECOND-STAGE DATA LATCH CIRCUIT
DATA OUTPUT FEEDBACK CLOCKS
DRAM INTERNAL DATA SIGNAL
527 RECEIVER CIRCUIT AND FIRST-STAGE DATA LATCH CIRCUIT
CLOCK
CLOCK REPRODUCTION AND PHASE ADJUSTING AND FREQUENCY MULTIPLIER CIRCUIT (DLL)
DQ
501 DOMAIN CROSSING CIRCUIT FROM WDPS PHASE TO CLOCK PHASE
COMMAND/ADDRESS RECEPTION FEEDBACK CLOCKS
DATA OUTPUT DRAM INTERNAL 0,90,180,270 -DEGREE PHASE CLOCKS
205
RECEPTION PHASE ADJUSTING SIGNAL
201
DQ OUTPUT DRIVER
206
208
0-DEGREE,180-DEGREE CLOCKS
531
COMMAND/ADDRESS
RECEPTION PHASE COMPARING CIRCUIT
RECEPTION REPLICA
COMMAND/ADDRESS RECEIVER

FIG.51

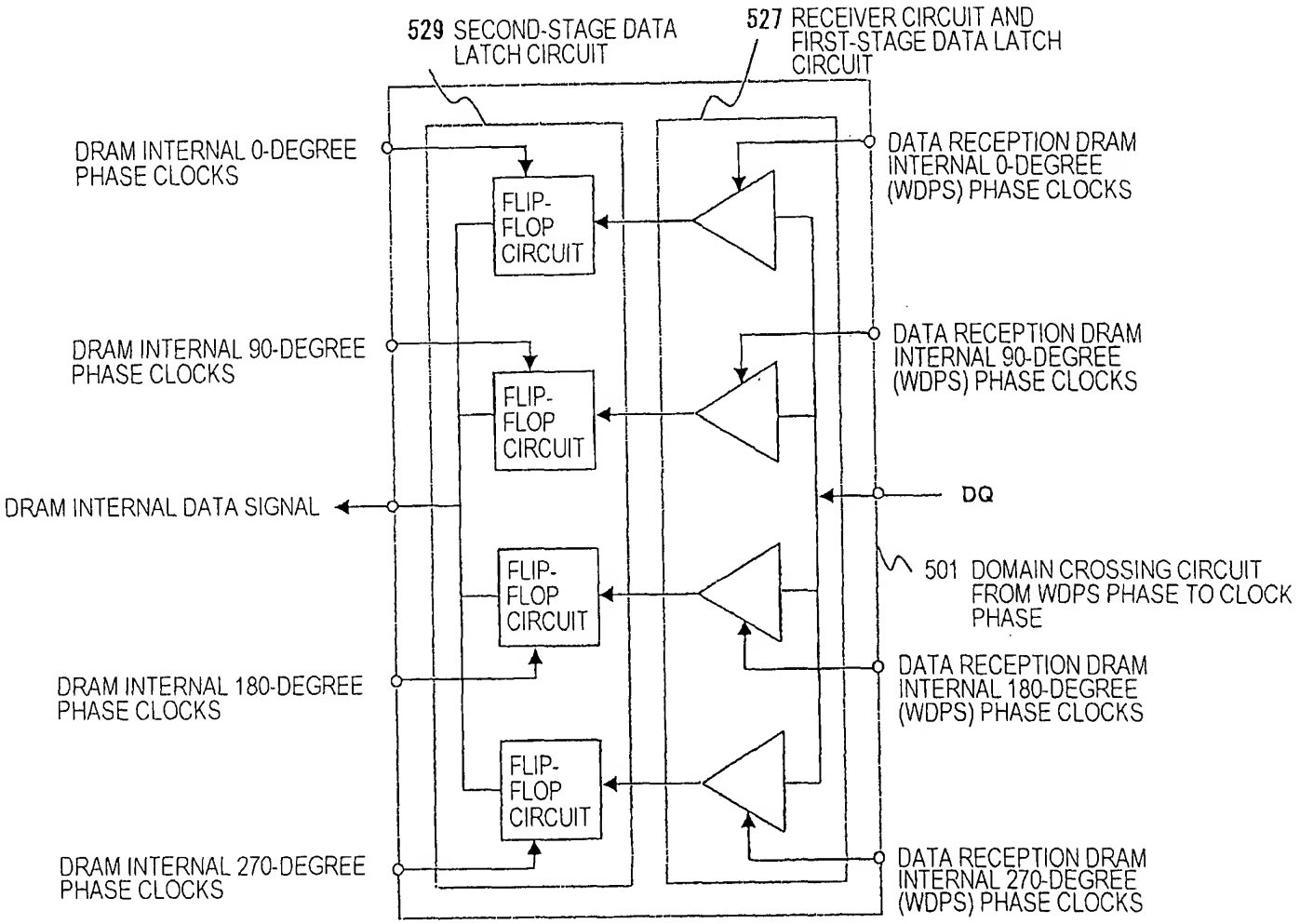

529 SECOND-STAGE DATA LATCH CIRCUIT
527 RECEIVER CIRCUIT AND FIRST-STAGE DATA LATCH CIRCUIT
DRAM INTERNAL 0-DEGREE PHASE CLOCKS
DRAM INTERNAL 90-DEGREE PHASE CLOCKS
DRAM INTERNAL DATA SIGNAL
DRAM INTERNAL 180-DEGREE PHASE CLOCKS
DRAM INTERNAL 270-DEGREE PHASE CLOCKS
FLIP-FLOP CIRCUIT
FLIP-FLOP CIRCUIT
FLIP-FLOP CIRCUIT
FLIP-FLOP CIRCUIT
DATA RECEPTION DRAM INTERNAL 0-DEGREE (WDPS) PHASE CLOCKS
DATA RECEPTION DRAM INTERNAL 90-DEGREE (WDPS) PHASE CLOCKS
DQ
501 DOMAIN CROSSING CIRCUIT FROM WDPS PHASE TO CLOCK PHASE
DATA RECEPTION DRAM INTERNAL 180-DEGREE (WDPS) PHASE CLOCKS
DATA RECEPTION DRAM INTERNAL 270-DEGREE (WDPS) PHASE CLOCKS

FIG. 52

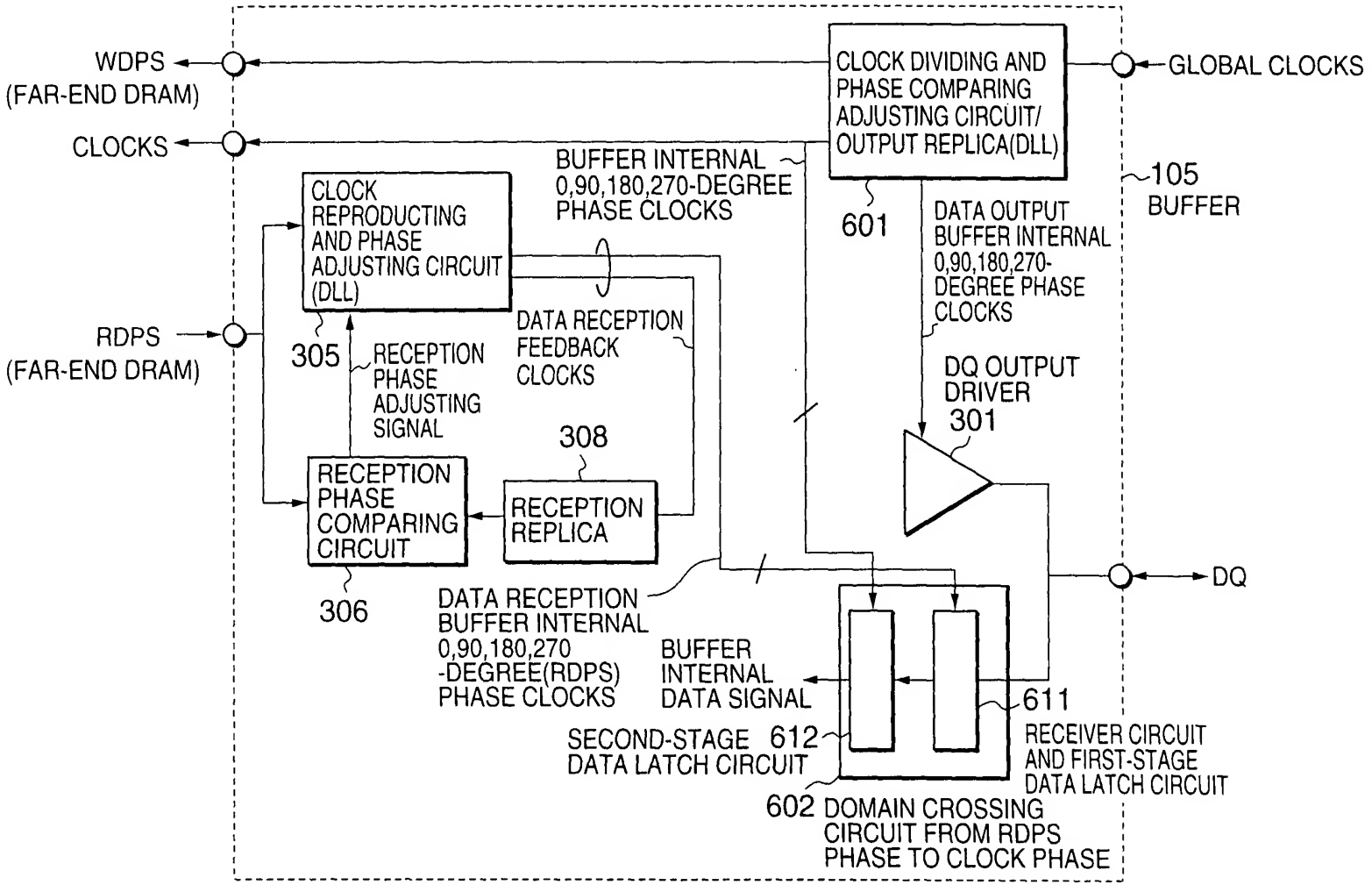

WDPS
(FAR-END DRAM)
CLOCKS
RDPS
(FAR-END DRAM)
CLOCK DIVIDING AND PHASE COMPARING ADJUSTING CIRCUIT/ OUTPUT REPLICA(DLL)
GLOBAL CLOCKS
105
BUFFER
601
BUFFER INTERNAL 0,90,180,270-DEGREE PHASE CLOCKS
DATA OUTPUT BUFFER INTERNAL 0,90,180,270-DEGREE PHASE CLOCKS
CLOCK REPRODUCTING AND PHASE ADJUSTING CIRCUIT (DLL)
305
RECEPTION PHASE ADJUSTING SIGNAL
DATA RECEPTION FEEDBACK CLOCKS
DQ OUTPUT DRIVER
301
308
RECEPTION PHASE COMPARING CIRCUIT
RECEPTION REPLICA
306
DQ
DATA RECEPTION BUFFER INTERNAL 0,90,180,270 -DEGREE(RDPS) PHASE CLOCKS
BUFFER INTERNAL DATA SIGNAL
611
SECOND-STAGE DATA LATCH CIRCUIT
612
RECEIVER CIRCUIT AND FIRST-STAGE DATA LATCH CIRCUIT
602
DOMAIN CROSSING CIRCUIT FROM RDPS PHASE TO CLOCK PHASE

FIG.53

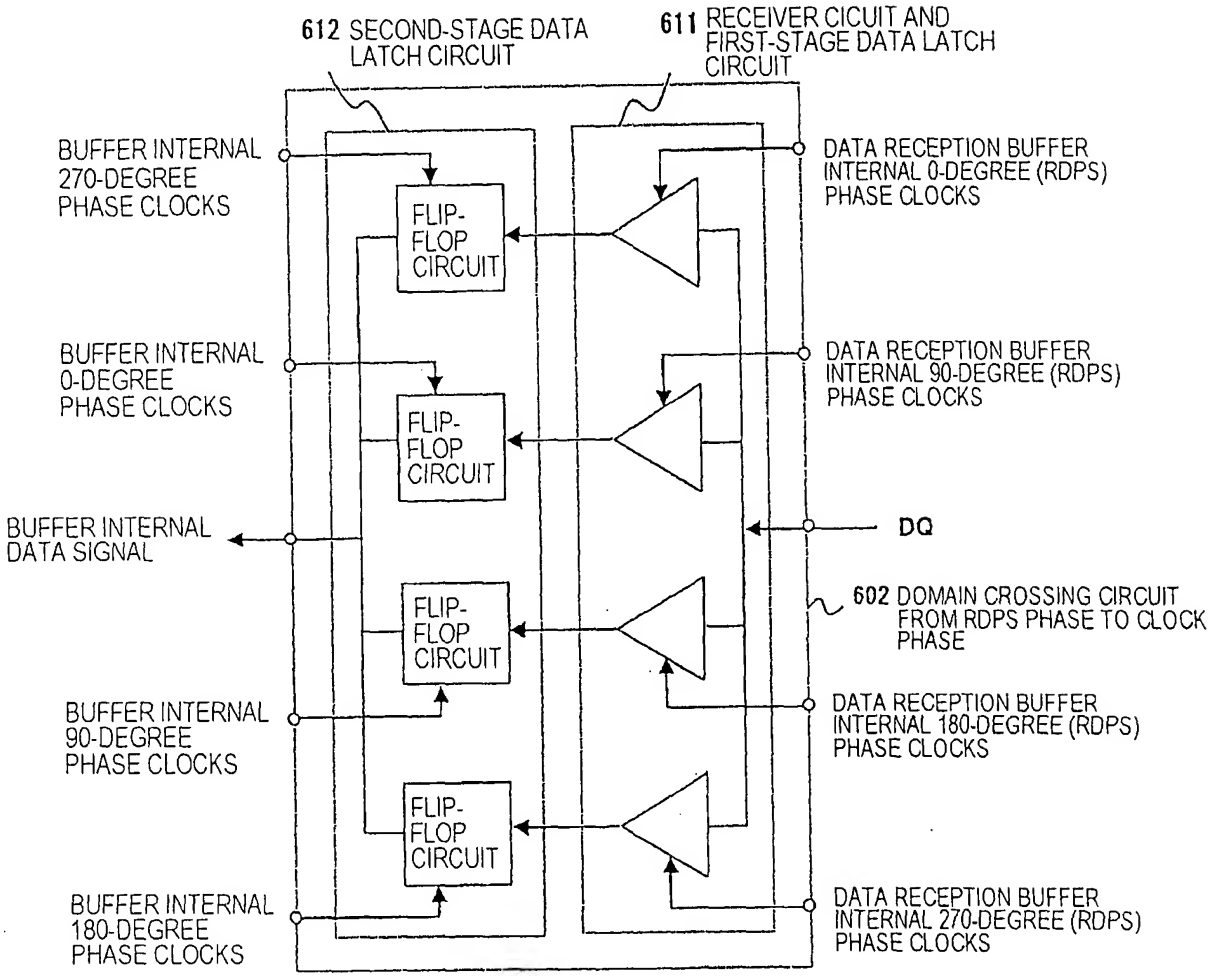

612 SECOND-STAGE DATA LATCH CIRCUIT
611 RECEIVER CICUIT AND FIRST-STAGE DATA LATCH CIRCUIT
BUFFER INTERNAL 270-DEGREE PHASE CLOCKS
BUFFER INTERNAL 0-DEGREE PHASE CLOCKS
BUFFER INTERNAL DATA SIGNAL
BUFFER INTERNAL 90-DEGREE PHASE CLOCKS
BUFFER INTERNAL 180-DEGREE PHASE CLOCKS
FLIP-FLOP CIRCUIT
FLIP-FLOP CIRCUIT
FLIP-FLOP CIRCUIT
FLIP-FLOP CIRCUIT
DATA RECEPTION BUFFER INTERNAL 0-DEGREE (RDPS) PHASE CLOCKS
DATA RECEPTION BUFFER INTERNAL 90-DEGREE (RDPS) PHASE CLOCKS
DQ
602 DOMAIN CROSSING CIRCUIT FROM RDPS PHASE TO CLOCK PHASE
DATA RECEPTION BUFFER INTERNAL 180-DEGREE (RDPS) PHASE CLOCKS
DATA RECEPTION BUFFER INTERNAL 270-DEGREE (RDPS) PHASE CLOCKS

FIG. 54

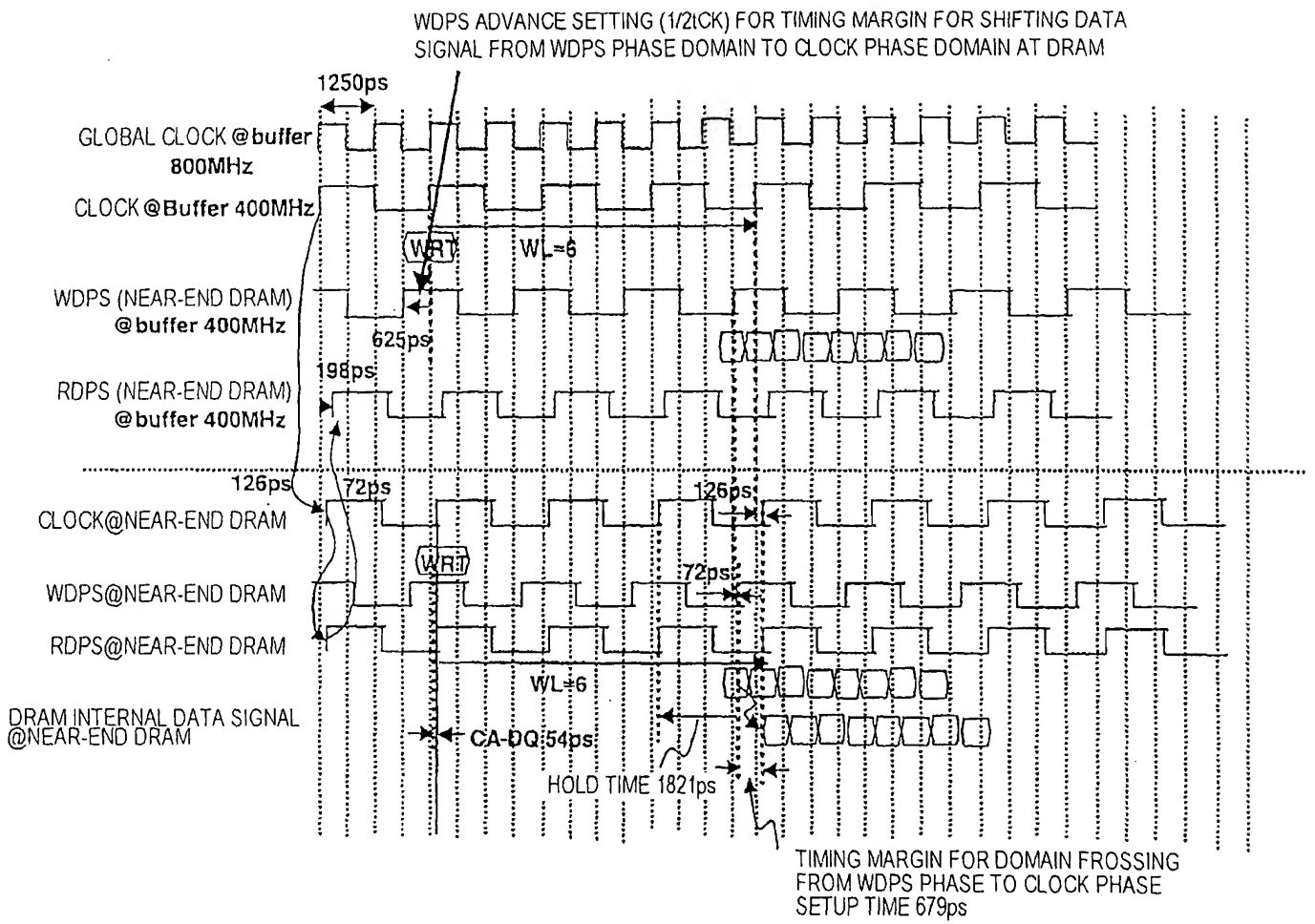

WDPS ADVANCE SETTING (1/2tCK) FOR TIMING MARGIN FOR SHIFTING DATA SIGNAL FROM WDPS PHASE DOMAIN TO CLOCK PHASE DOMAIN AT DRAM
1250ps
GLOBAL CLOCK @buffer 800MHz
CLOCK @Buffer 400MHz
WRT
WL=6
WDPS (NEAR-END DRAM) @buffer 400MHz
625ps
198ps
RDPS (NEAR-END DRAM) @buffer 400MHz
126ps
72ps
126ps
CLOCK@NEAR-END DRAM
WRT
72ps
WDPS@NEAR-END DRAM
RDPS@NEAR-END DRAM
WL=6
DRAM INTERNAL DATA SIGNAL @NEAR-END DRAM
CA-DQ 54ps
HOLD TIME 1821ps
TIMING MARGIN FOR DOMAIN FROSSING FROM WDPS PHASE TO CLOCK PHASE SETUP TIME 679ps

FIG. 55

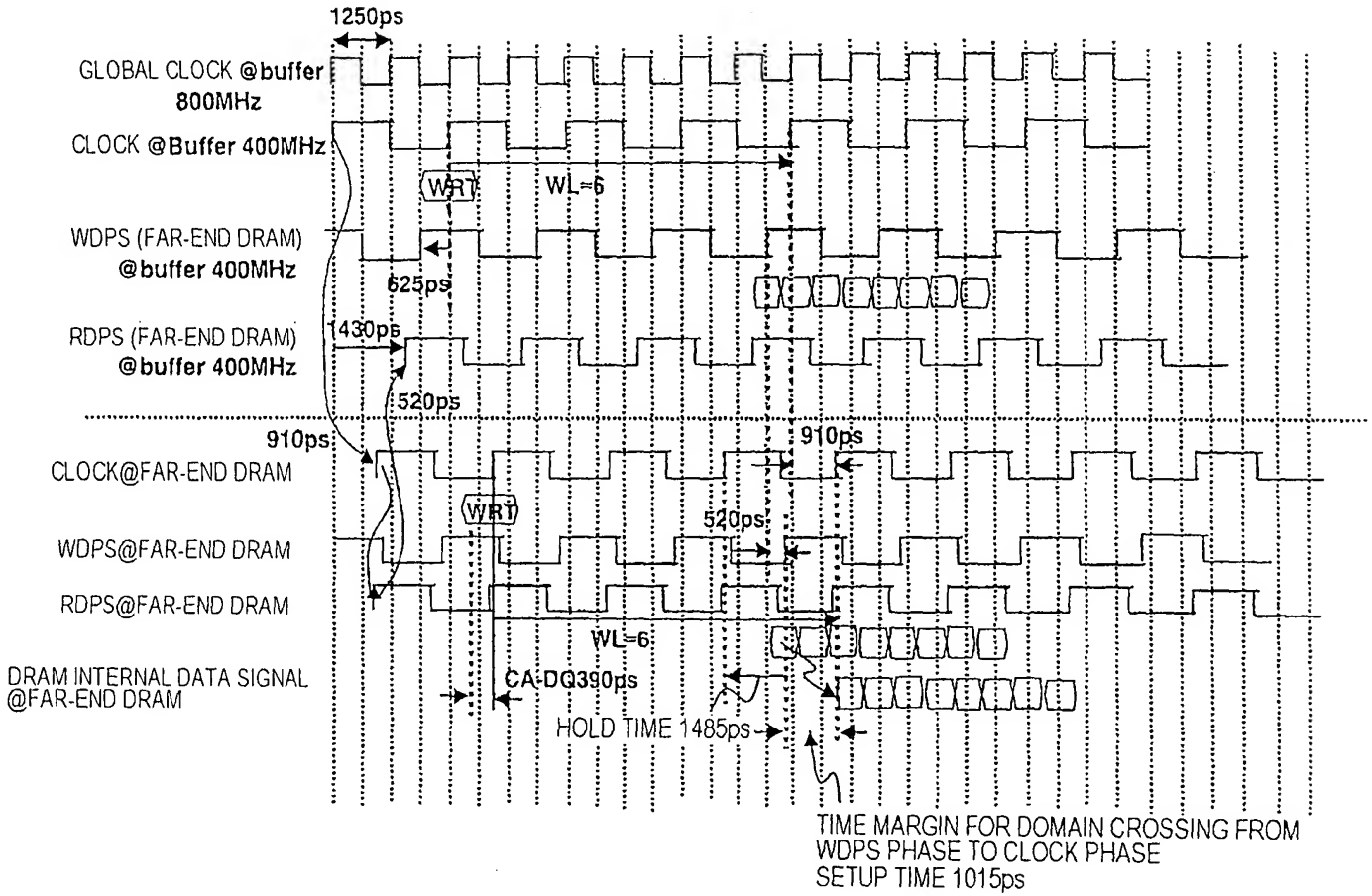

1250ps
GLOBAL CLOCK @buffer 800MHz
CLOCK @Buffer 400MHz
WRT
WL=6
WDPS (FAR-END DRAM) @buffer 400MHz
625ps
RDPS (FAR-END DRAM) @buffer 400MHz
1430ps
520ps
910ps
910ps
CLOCK@FAR-END DRAM
WRT
520ps
WDPS@FAR-END DRAM
RDPS@FAR-END DRAM
WL=6
DRAM INTERNAL DATA SIGNAL @FAR-END DRAM
CA-DQ390ps
HOLD TIME 1485ps
TIME MARGIN FOR DOMAIN CROSSING FROM WDPS PHASE TO CLOCK PHASE SETUP TIME 1015ps

FIG. 56

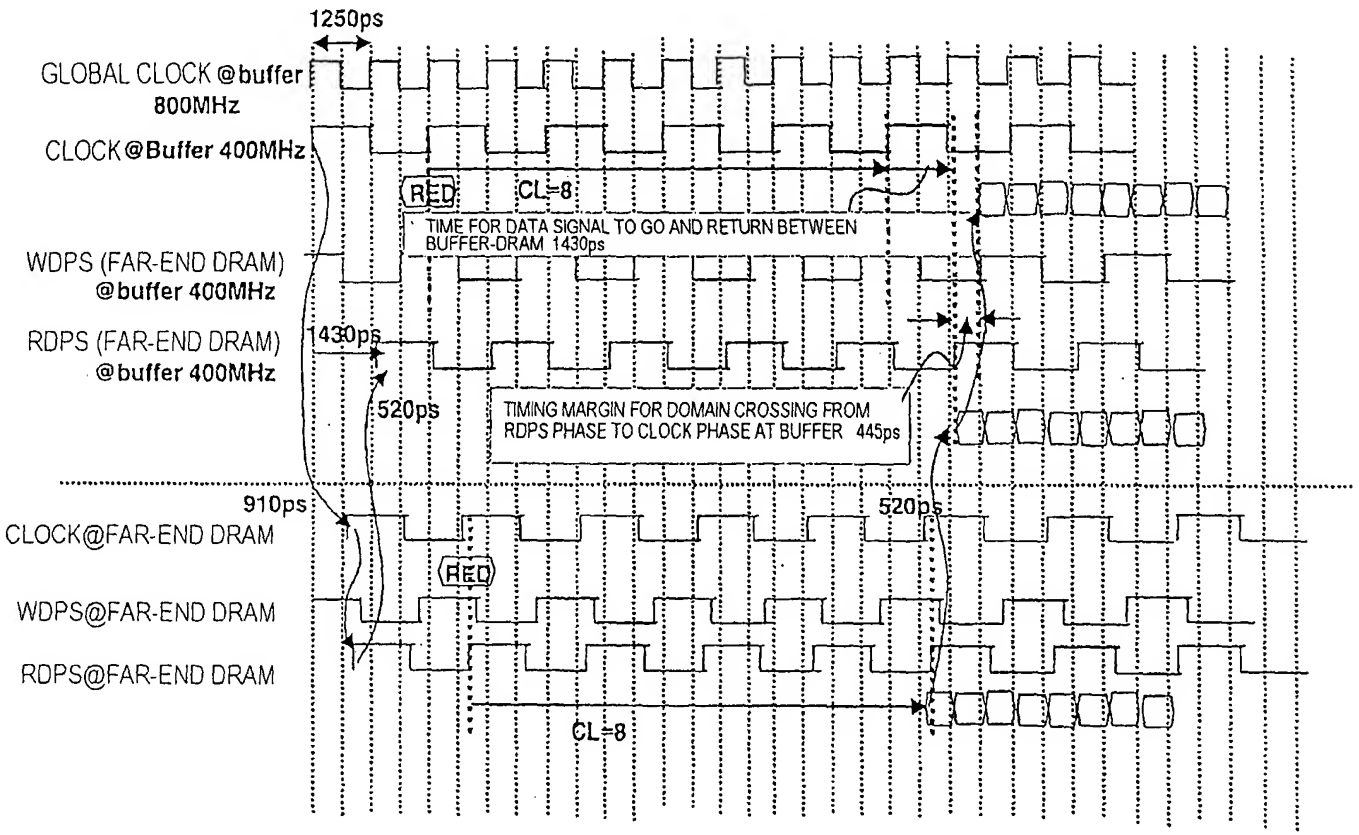

1250ps
GLOBAL CLOCK @buffer 800MHz
CLOCK@Buffer 400MHz
RED
CL=8
TIME FOR DATA SIGNAL TO GO AND RETURN BETWEEN BUFFER-DRAM 1430ps
WDPS (FAR-END DRAM) @buffer 400MHz
RDPS (FAR-END DRAM) @buffer 400MHz
1430ps
520ps
TIMING MARGIN FOR DOMAIN CROSSING FROM RDPS PHASE TO CLOCK PHASE AT BUFFER 445ps
910ps
520ps
CLOCK@FAR-END DRAM
RED
WDPS@FAR-END DRAM
RDPS@FAR-END DRAM
CL=8

FIG. 57

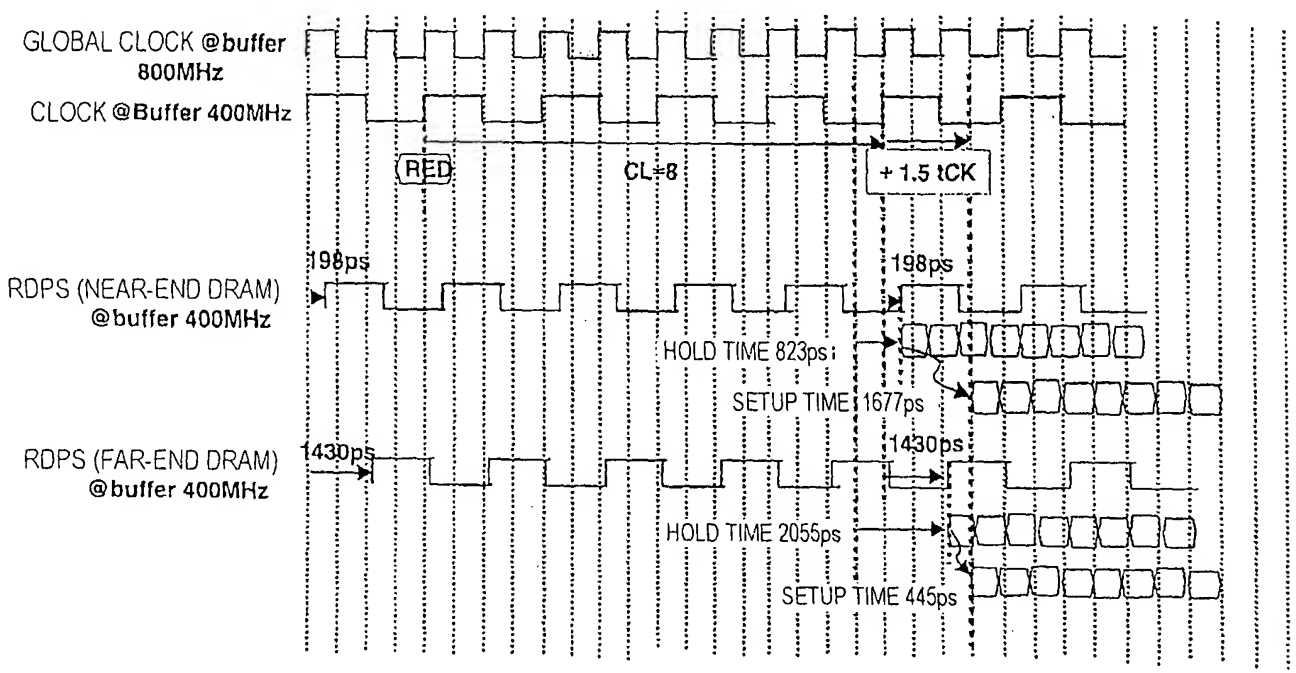

GLOBAL CLOCK @buffer 800MHz
CLOCK @Buffer 400MHz
RED
CL=8
+ 1.5 tCK
198ps
198ps
RDPS (NEAR-END DRAM) @buffer 400MHz
HOLD TIME 823ps
SETUP TIME 1677ps
1430ps
1430ps
RDPS (FAR-END DRAM) @buffer 400MHz
HOLD TIME 2055ps
SETUP TIME 445ps

FIG. 58

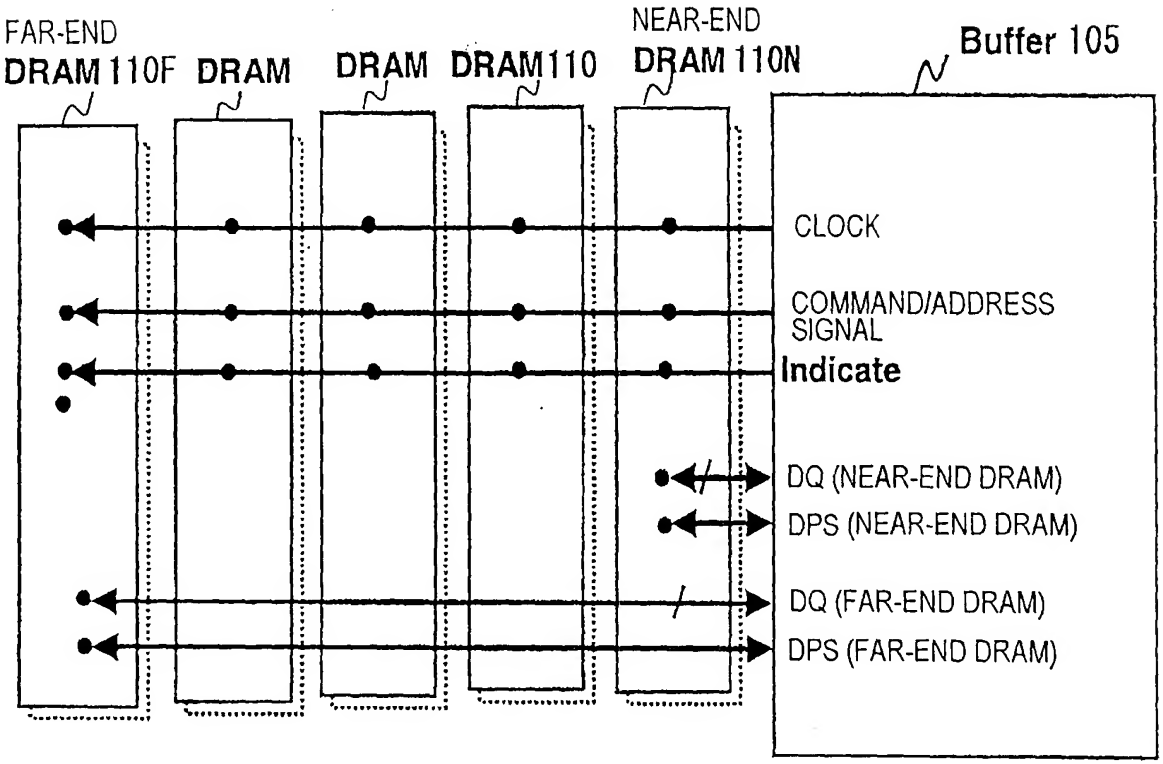

FAR-END
DRAM 110F
DRAM
DRAM
DRAM110
NEAR-END
DRAM 110N
Buffer 105
CLOCK
COMMAND/ADDRESS SIGNAL
Indicate
DQ (NEAR-END DRAM)
DPS (NEAR-END DRAM)
DQ (FAR-END DRAM)
DPS (FAR-END DRAM)

FIG. 59

103

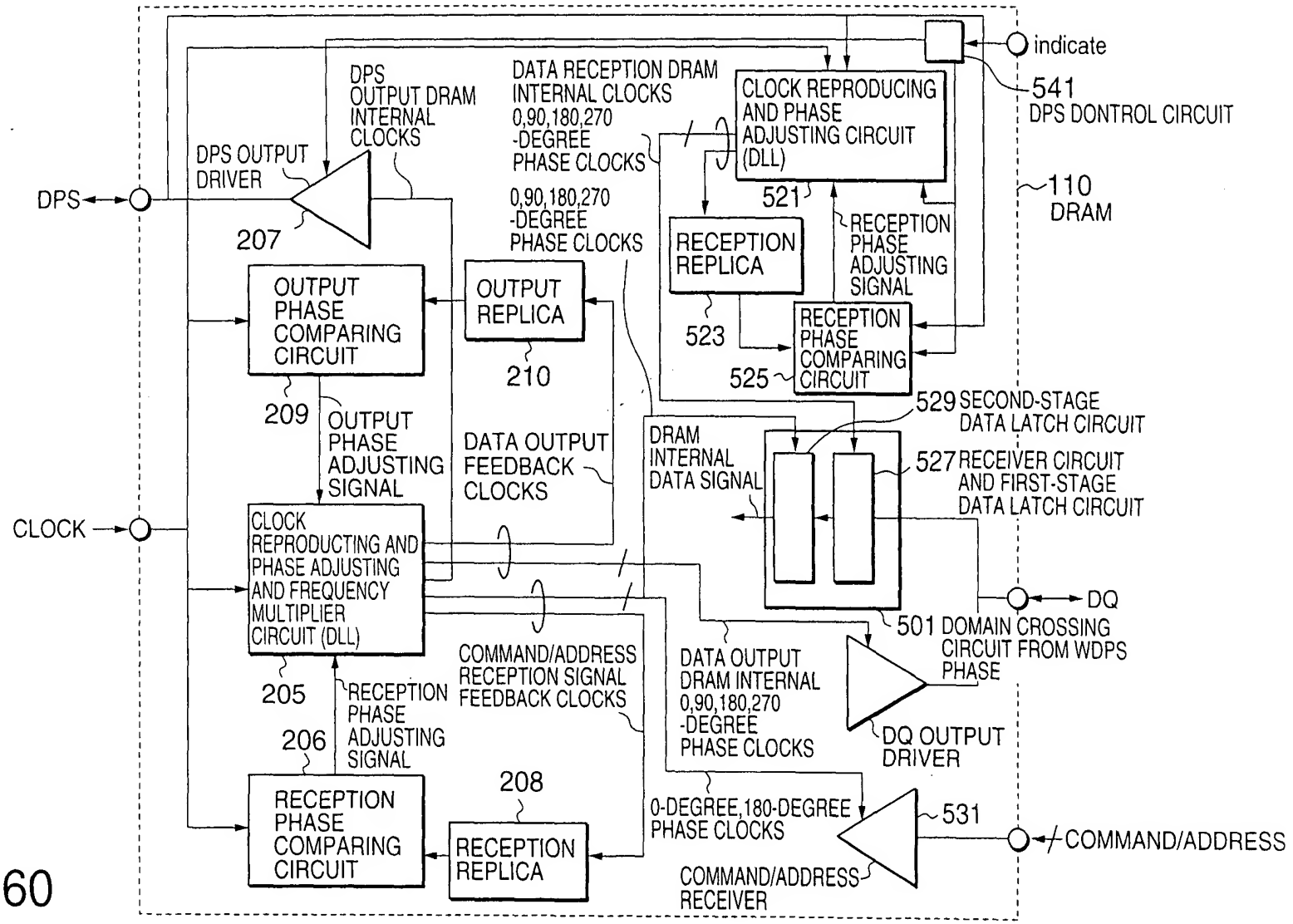

indicate
541
DPS DONTROL CIRCUIT
DPS OUTPUT DRAM INTERNAL CLOCKS
DATA RECEPTION DRAM INTERNAL CLOCKS 0,90,180,270 -DEGREE PHASE CLOCKS
CLOCK REPRODUCING AND PHASE ADJUSTING CIRCUIT (DLL)
521
110
DRAM
DPS
DPS OUTPUT DRIVER
207
0,90,180,270 -DEGREE PHASE CLOCKS
RECEPTION REPLICA
RECEPTION PHASE ADJUSTING SIGNAL
OUTPUT PHASE COMPARING CIRCUIT
OUTPUT REPLICA
523
RECEPTION PHASE COMPARING CIRCUIT
525
210
529 SECOND-STAGE DATA LATCH CIRCUIT
209
OUTPUT PHASE ADJUSTING SIGNAL
DATA OUTPUT FEEDBACK CLOCKS
DRAM INTERNAL DATA SIGNAL
527 RECEIVER CIRCUIT AND FIRST-STAGE DATA LATCH CIRCUIT
CLOCK
CLOCK REPRODUCTING AND PHASE ADJUSTING AND FREQUENCY MULTIPLIER CIRCUIT (DLL)
DQ
501 DOMAIN CROSSING CIRCUIT FROM WDPS PHASE
COMMAND/ADDRESS RECEPTION SIGNAL FEEDBACK CLOCKS
DATA OUTPUT DRAM INTERNAL 0,90,180,270 -DEGREE PHASE CLOCKS
205
RECEPTION PHASE ADJUSTING SIGNAL
206
DQ OUTPUT DRIVER
208
0-DEGREE,180-DEGREE PHASE CLOCKS
531
RECEPTION PHASE COMPARING CIRCUIT
RECEPTION REPLICA
COMMAND/ADDRESS
COMMAND/ADDRESS RECEIVER

FIG.60

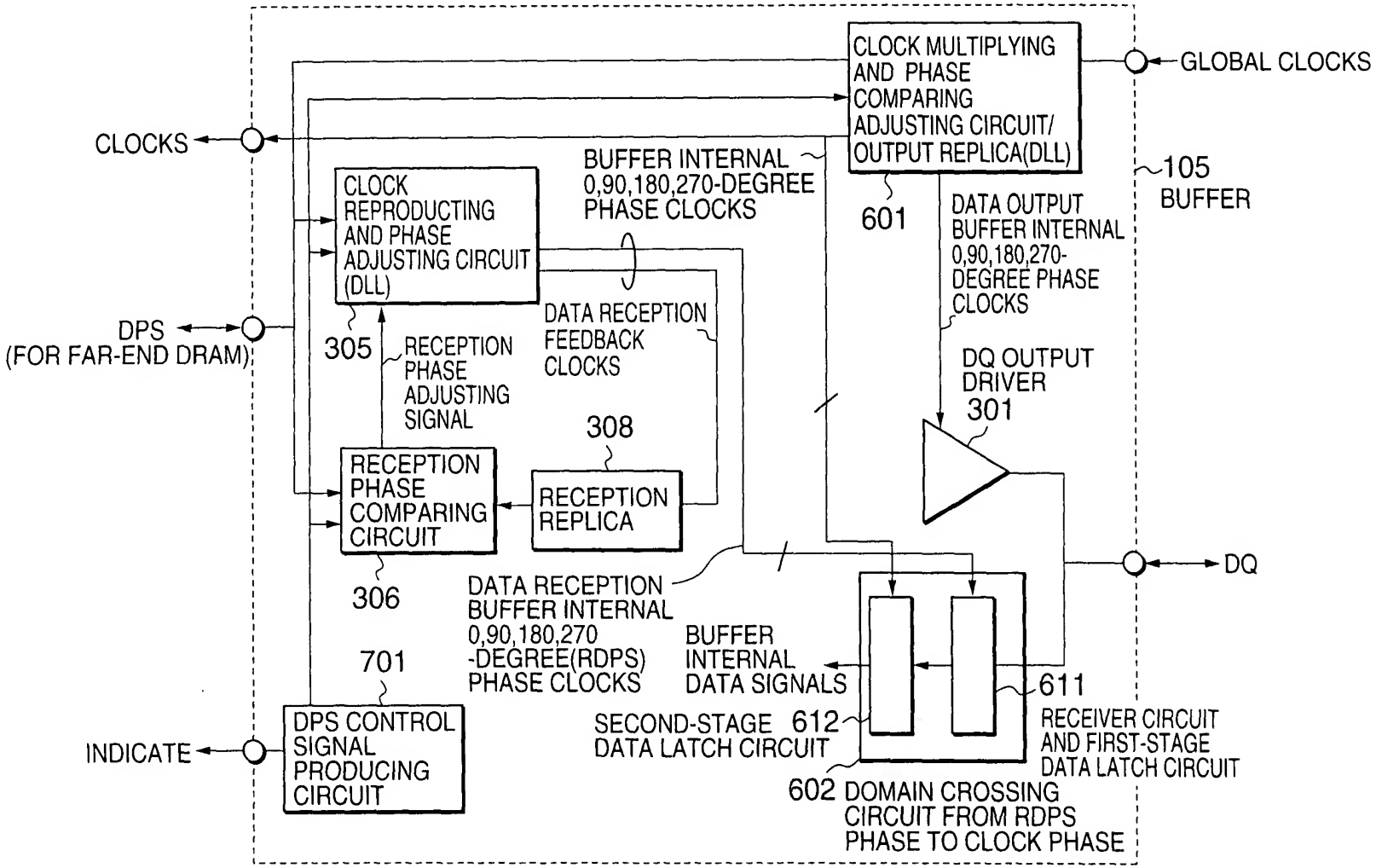

CLOCK MULTIPLYING AND PHASE COMPARING ADJUSTING CIRCUIT/ OUTPUT REPLICA(DLL)
GLOBAL CLOCKS
CLOCKS
BUFFER INTERNAL 0,90,180,270-DEGREE PHASE CLOCKS
601
105 BUFFER
DATA OUTPUT BUFFER INTERNAL 0,90,180,270-DEGREE PHASE CLOCKS
CLOCK REPRODUCTING AND PHASE ADJUSTING CIRCUIT (DLL)
DPS (FOR FAR-END DRAM)
305
RECEPTION PHASE ADJUSTING SIGNAL
DATA RECEPTION FEEDBACK CLOCKS
DQ OUTPUT DRIVER
301
308
RECEPTION PHASE COMPARING CIRCUIT
RECEPTION REPLICA
DQ
306
DATA RECEPTION BUFFER INTERNAL 0,90,180,270 -DEGREE(RDPS) PHASE CLOCKS
BUFFER INTERNAL DATA SIGNALS
701
611
SECOND-STAGE DATA LATCH CIRCUIT
612
RECEIVER CIRCUIT AND FIRST-STAGE DATA LATCH CIRCUIT
INDICATE
DPS CONTROL SIGNAL PRODUCING CIRCUIT
602 DOMAIN CROSSING CIRCUIT FROM RDPS PHASE TO CLOCK PHASE

FIG.61

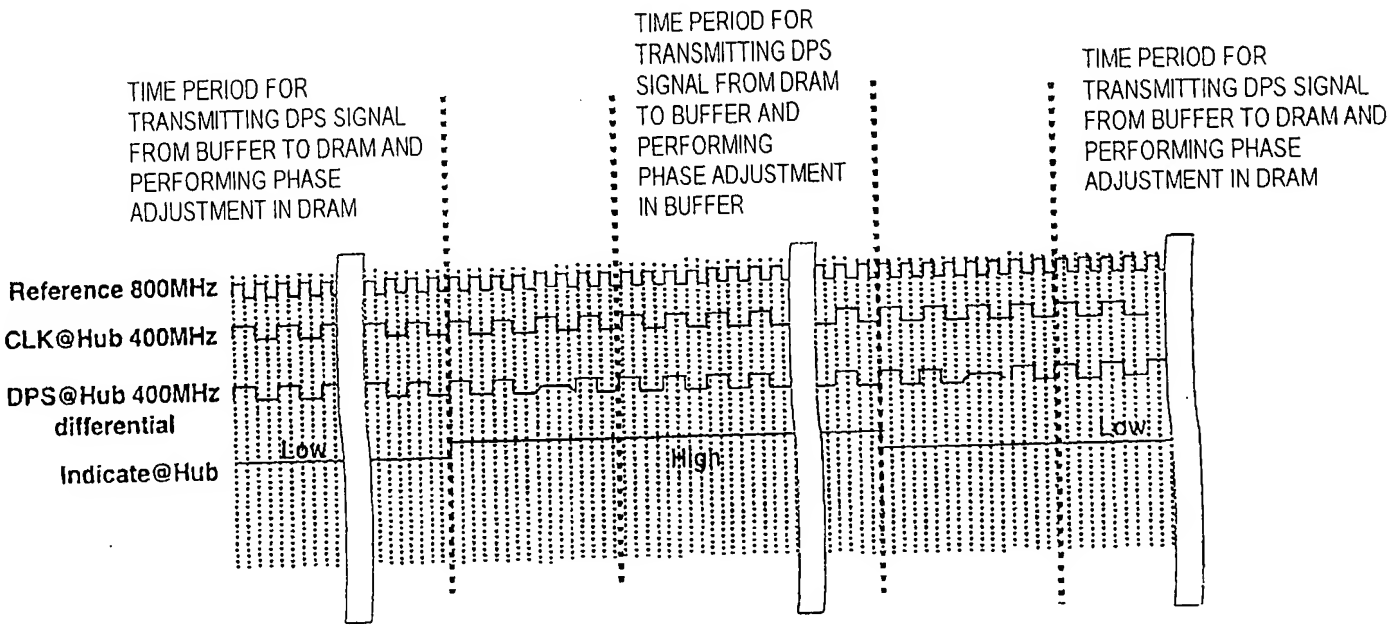

TIME PERIOD FOR TRANSMITTING DPS SIGNAL FROM BUFFER TO DRAM AND PERFORMING PHASE ADJUSTMENT IN DRAM
TIME PERIOD FOR TRANSMITTING DPS SIGNAL FROM DRAM TO BUFFER AND PERFORMING PHASE ADJUSTMENT IN BUFFER
TIME PERIOD FOR TRANSMITTING DPS SIGNAL FROM BUFFER TO DRAM AND PERFORMING PHASE ADJUSTMENT IN DRAM
Reference 800MHz
CLK@Hub 400MHz
DPS@Hub 400MHz differential
Indicate@Hub
Low
High
Low

FIG. 62

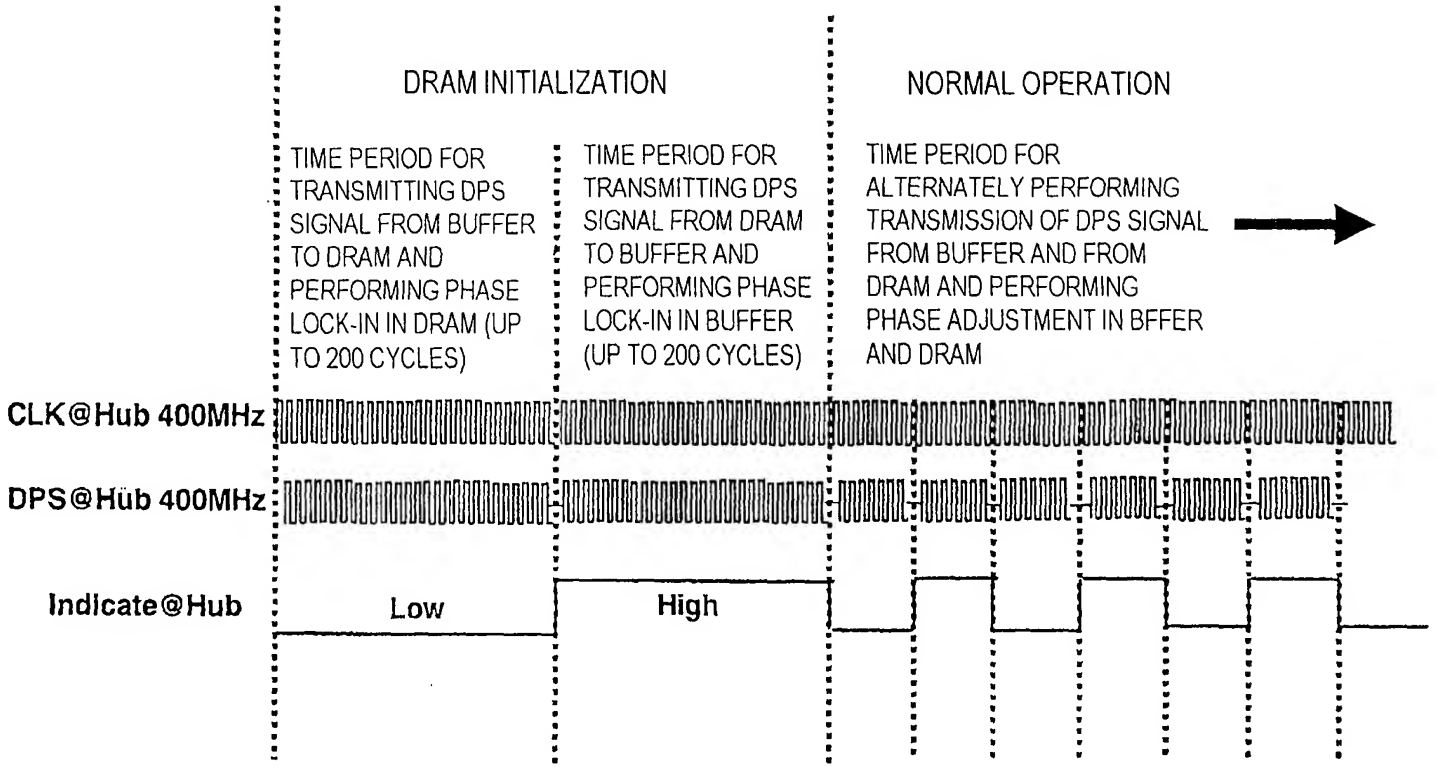

DRAM INITIALIZATION
NORMAL OPERATION
TIME PERIOD FOR TRANSMITTING DPS SIGNAL FROM BUFFER TO DRAM AND PERFORMING PHASE LOCK-IN IN DRAM (UP TO 200 CYCLES)
TIME PERIOD FOR TRANSMITTING DPS SIGNAL FROM DRAM TO BUFFER AND PERFORMING PHASE LOCK-IN IN BUFFER (UP TO 200 CYCLES)
TIME PERIOD FOR ALTERNATELY PERFORMING TRANSMISSION OF DPS SIGNAL FROM BUFFER AND FROM DRAM AND PERFORMING PHASE ADJUSTMENT IN BFFER AND DRAM
CLK@Hub 400MHz
DPS@Hub 400MHz
Indicate@Hub
Low
High

FIG. 63

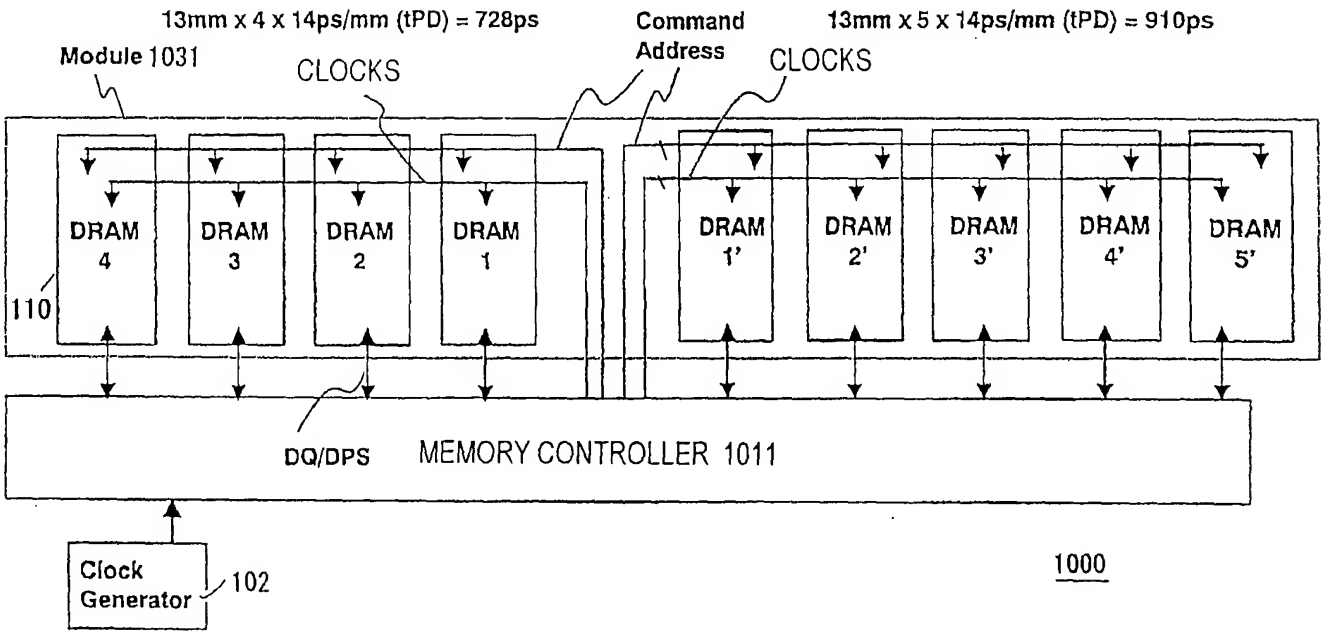

13mm x 4 x 14ps/mm (tPD) = 728ps
Command
Address
13mm x 5 x 14ps/mm (tPD) = 910ps
Module 1031
CLOCKS
CLOCKS
DRAM 4
DRAM 3
DRAM 2
DRAM 1
DRAM 1'
DRAM 2'
DRAM 3'
DRAM 4'
DRAM 5'
110
DQ/DPS
MEMORY CONTROLLER 1011
Clock Generator
102
1000

FIG. 64

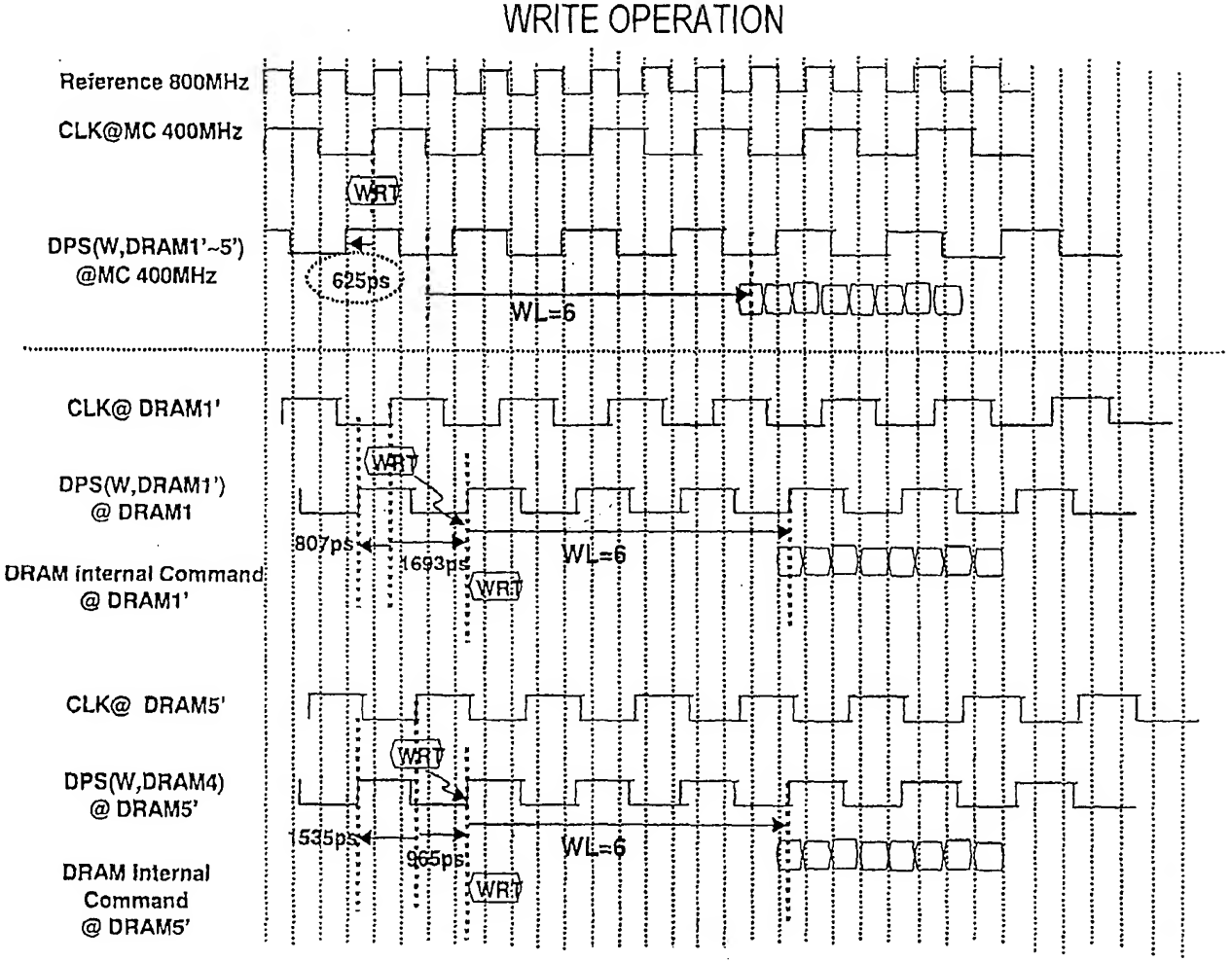

WRITE OPERATION
Reference 800MHz
CLK@MC 400MHz
WRT
DPS(W,DRAM1'~5')
@MC 400MHz
625ps
WL=6
CLK@ DRAM1'
WRT
DPS(W,DRAM1')
@ DRAM1
807ps
1693ps
WL=6
DRAM internal Command
@ DRAM1'
WRT
CLK@ DRAM5'
WRT
DPS(W,DRAM4)
@ DRAM5'
1535ps
965ps
WL=6
DRAM Internal
Command
@ DRAM5'
WRT

FIG. 65

READ OPERATION

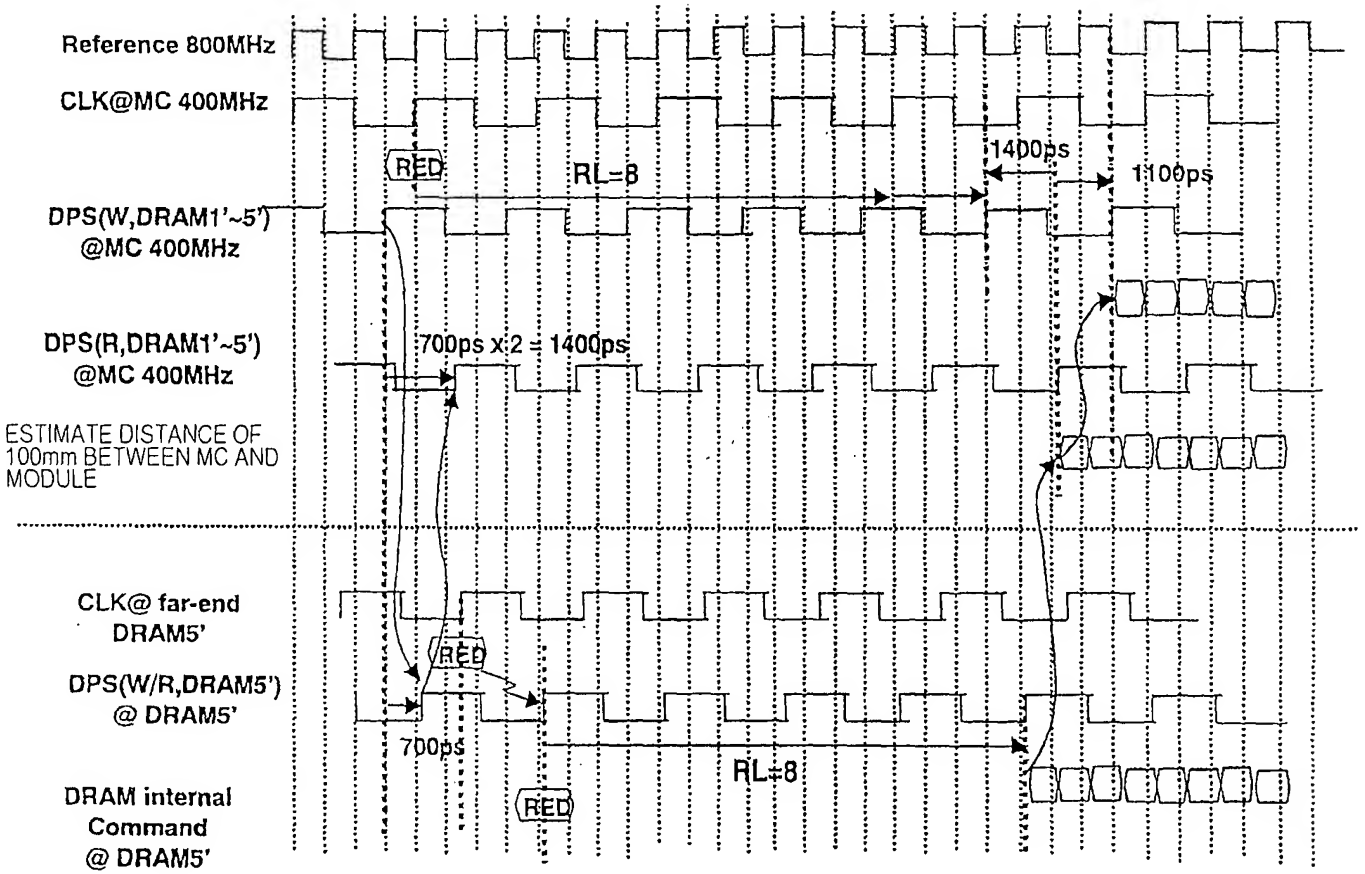


FIG. 66

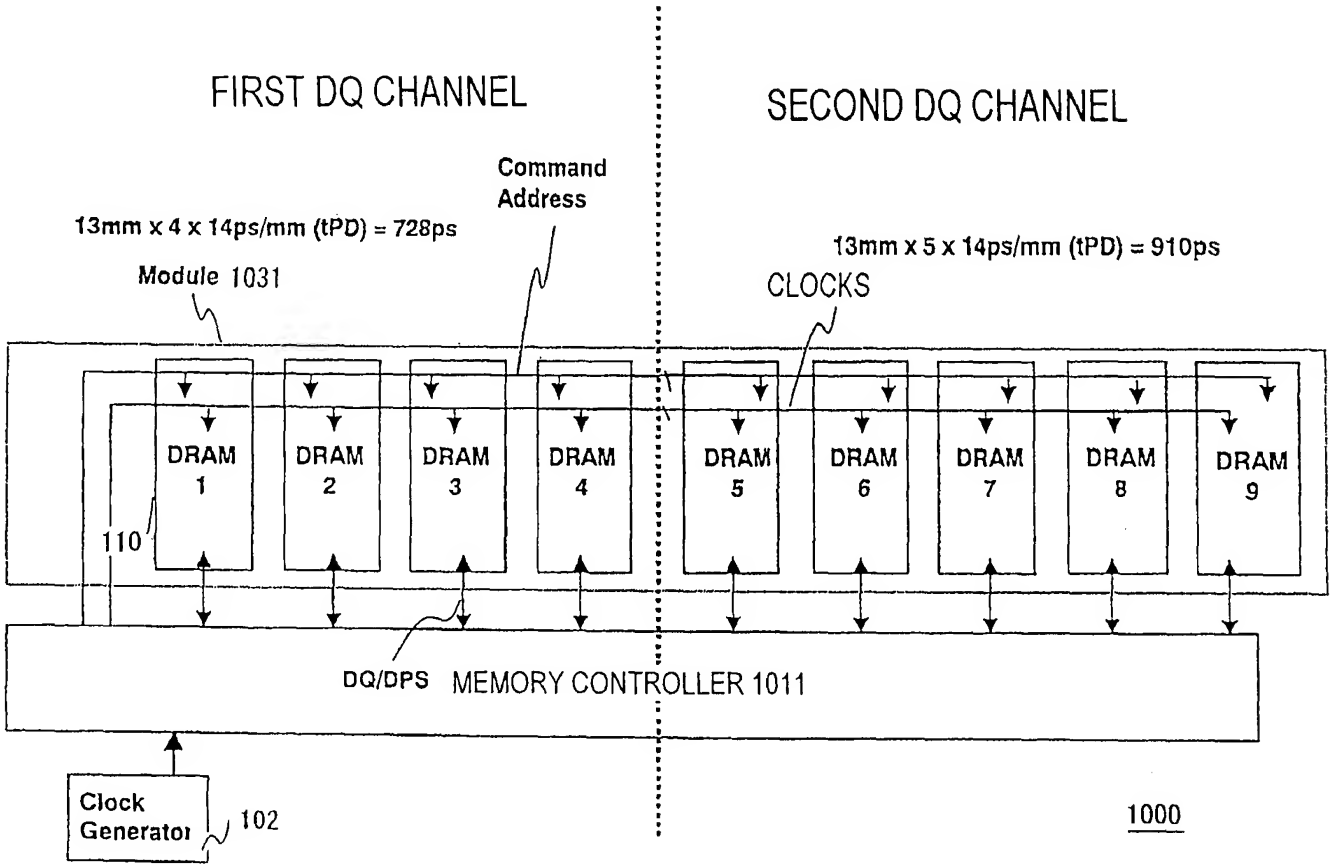

FIRST DQ CHANNEL
SECOND DQ CHANNEL
Command
Address
13mm x 4 x 14ps/mm (tPD) = 728ps
13mm x 5 x 14ps/mm (tPD) = 910ps
Module 1031
CLOCKS
DRAM 1
DRAM 2
DRAM 3
DRAM 4
DRAM 5
DRAM 6
DRAM 7
DRAM 8
DRAM 9
110
DQ/DPS
MEMORY CONTROLLER 1011
Clock Generator
102
1000

FIG. 67

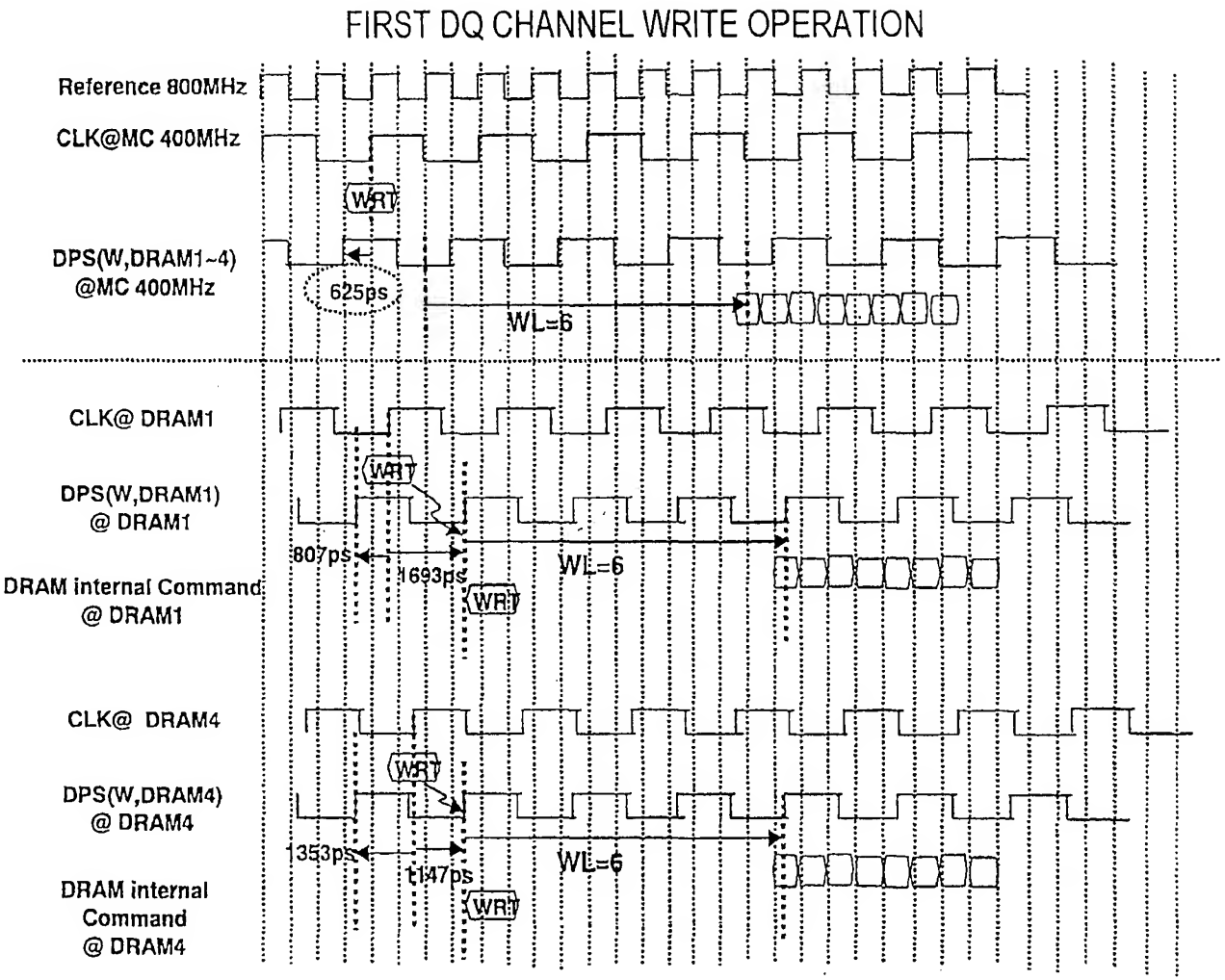

FIRST DQ CHANNEL WRITE OPERATION
Reference 800MHz
CLK@MC 400MHz
WRT
DPS(W,DRAM1~4)
@MC 400MHz
625ps
WL=6
CLK@ DRAM1
WRT
DPS(W,DRAM1)
@ DRAM1
807ps
1693ps
WL=6
DRAM internal Command
@ DRAM1
WRT
CLK@ DRAM4
WRT
DPS(W,DRAM4)
@ DRAM4
1353ps
1147ps
WL=6
DRAM internal
Command
@ DRAM4
WRT

FIG. 68

FIRST DQ CHANNEL READ OPERATION

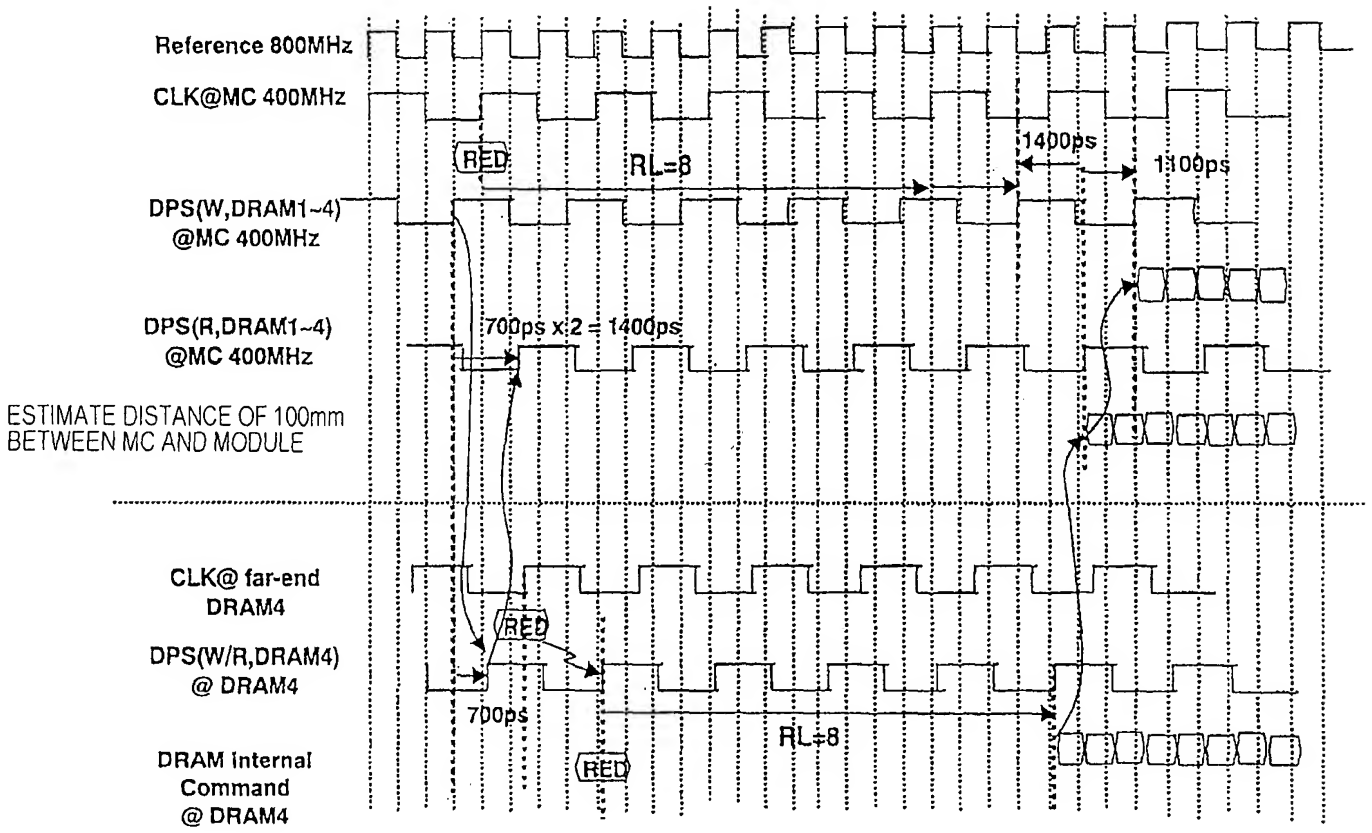


FIG. 69

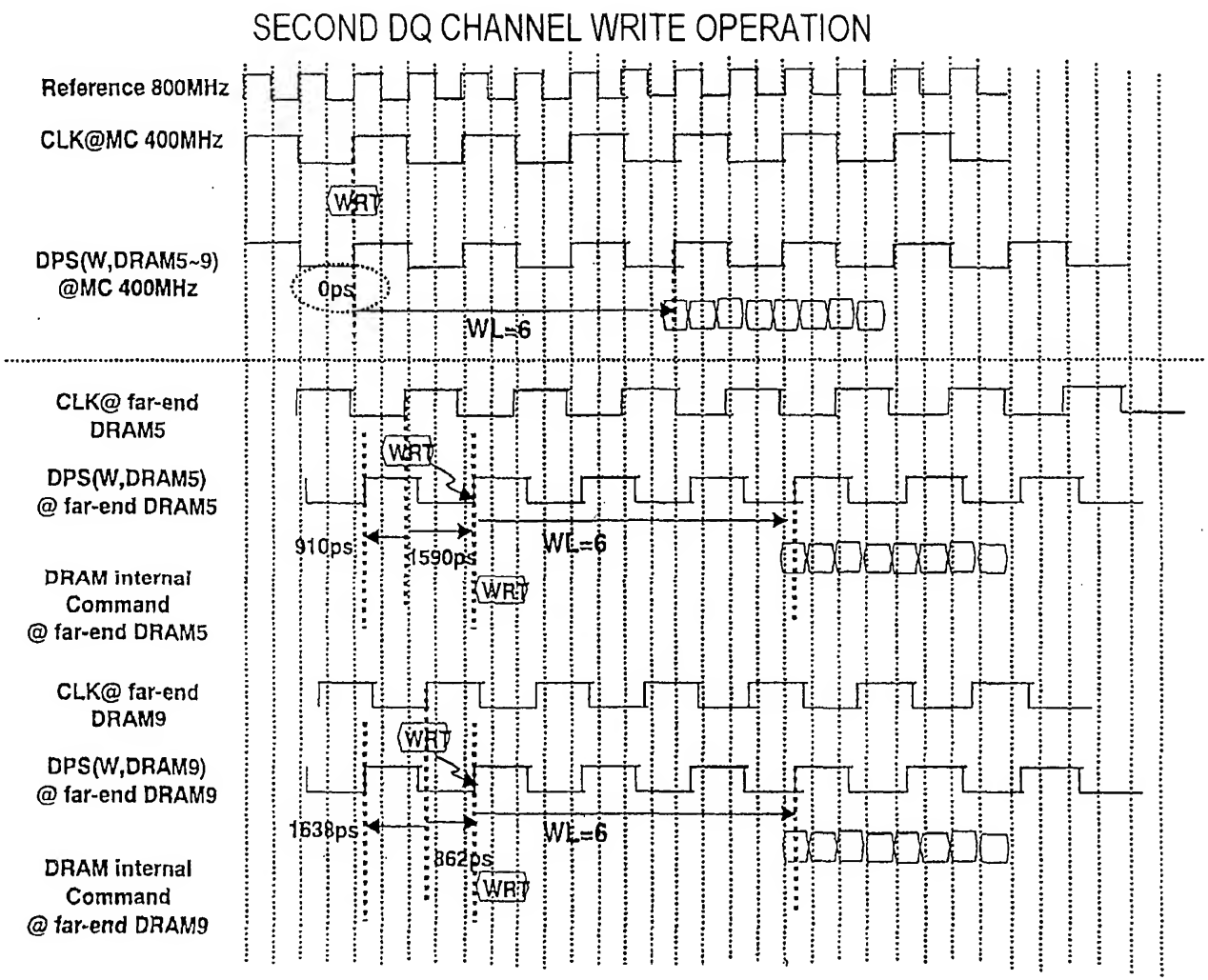

SECOND DQ CHANNEL WRITE OPERATION
Reference 800MHz
CLK@MC 400MHz
WRT
DPS(W,DRAM5~9)
@MC 400MHz
0ps
WL=6
CLK@ far-end
DRAM5
WRT
DPS(W,DRAM5)
@ far-end DRAM5
910ps
1590ps
WL=6
DRAM internal
Command
@ far-end DRAM5
WRT
CLK@ far-end
DRAM9
WRT
DPS(W,DRAM9)
@ far-end DRAM9
1638ps
WL=6
862ps
DRAM internal
Command
@ far-end DRAM9
WRT

FIG. 70

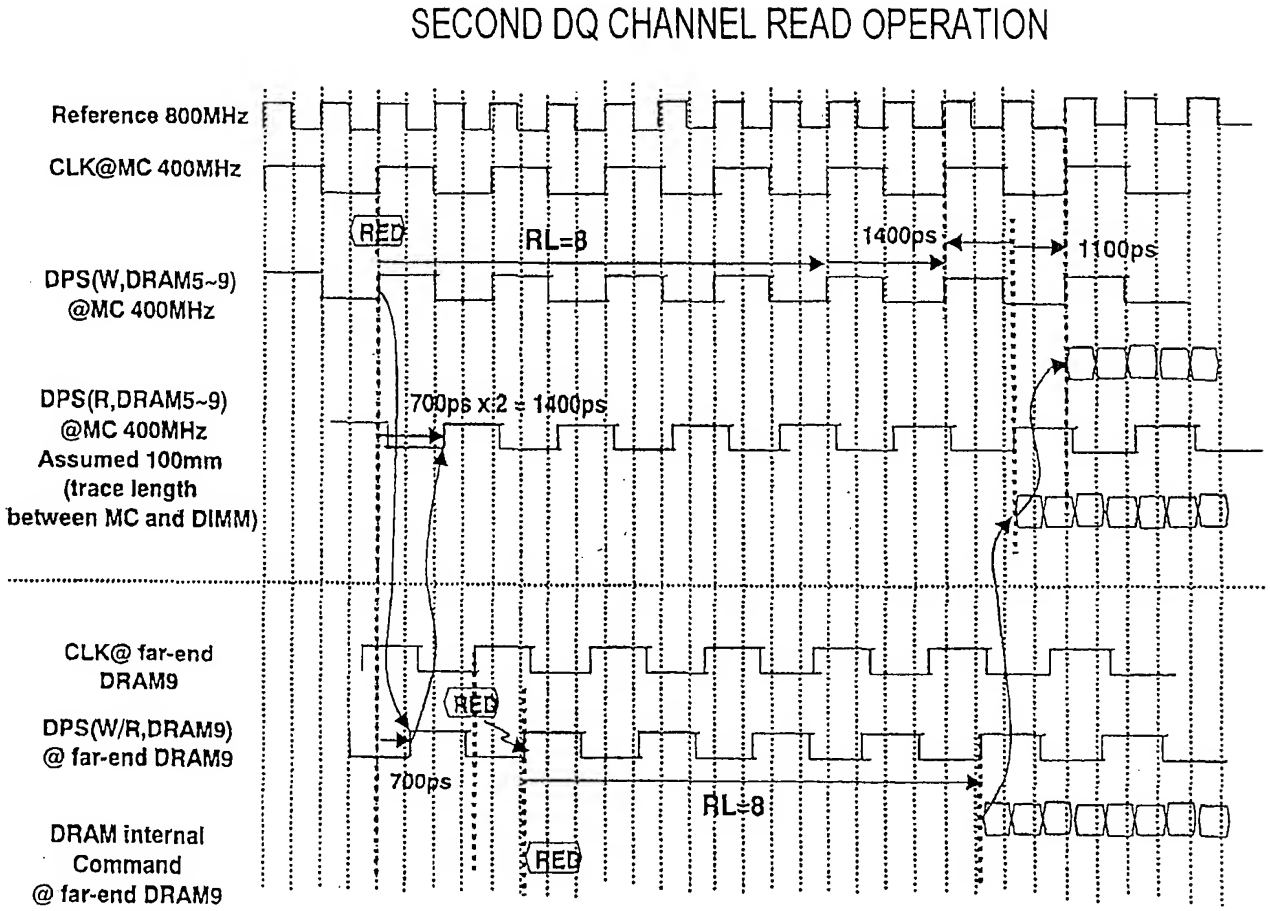

SECOND DQ CHANNEL READ OPERATION
Reference 800MHz
CLK@MC 400MHz
RED
RL=8
1400ps
1100ps
DPS(W,DRAM5~9)
@MC 400MHz
DPS(R,DRAM5~9)
@MC 400MHz
Assumed 100mm
(trace length
between MC and DIMM)
700ps x 2 = 1400ps
CLK@ far-end
DRAM9
RED
DPS(W/R,DRAM9)
@ far-end DRAM9
700ps
RL=8
DRAM internal
Command
@ far-end DRAM9
RED

FIG. 71